An Instruction Manual

on

Basic Electronics

Network of Instrument Technical personnel
and User scientists of Bangladesh (NITUB)

An Instruction Manual on

Basic Electronics

Author

Dr. Md. Habibur Rahman
Professor
Department of Electrical & Electronic Engineering
University of Dhaka
Dhaka-1000, Bangladesh

Reviewer

Dr. Rezaul Karim Mazumder
Former Professor
Department of Electrical & Electronic Engineering
University of Dhaka
Dhaka-1000, Bangladesh

Sponsor

International Science Programme (ISP)
Uppsala University, Sweden

Published by

Network of Instrument Technical personnel and User scientists of Bangladesh (NITUB)

Printed by

DS Printing and Packaging
243/D New Elephant Road, Dhaka
E-mail: adspp016@gmail.com

Contents

CHAPTER 1

Basic Concepts for Electronics

1.1 Introduction

Currently, we people live in an era of developed engineering and technology mainly Electrical and Electronics Engineering. In today's world, people cannot think of their lives without mobile phone, television, computer and other devices that have made our lives easy and enjoyable. These devices are the gift of Electrical and Electronics Engineering. All of them work based on the flow of charges. As this souvenir is made for non electrical engineers, before going to the main topics, it is necessary to explain some terms related to electrical and electronic circuits. A ***circuit*** is a complete path through which charge flows. Professionals of different fields study electronics. The prerequisites to study electronics are DC/AC circuit courses, Electricity and magnetism, algebra, and some trigonometry. Basic Electronics provides understanding of construction, operation, testing of semiconductor devices and the circuits in which they are used. As the targeted readers of this Manual are not directly from electrical fields, we will discuss some important concepts necessary to understand electronics.

1.2 Symbols Used in Electronics

The electronic circuits are constructed using semiconductor devices, power sources, switches etc. In schematic diagrams of circuits, all these components are represented by their symbols. Some very common symbols are given in Fig.1-1. Although, we do not require memorizing all of them, we can use them if required for further studies/applications.

Common Symbols Used in Electrical and Electronics Circuits

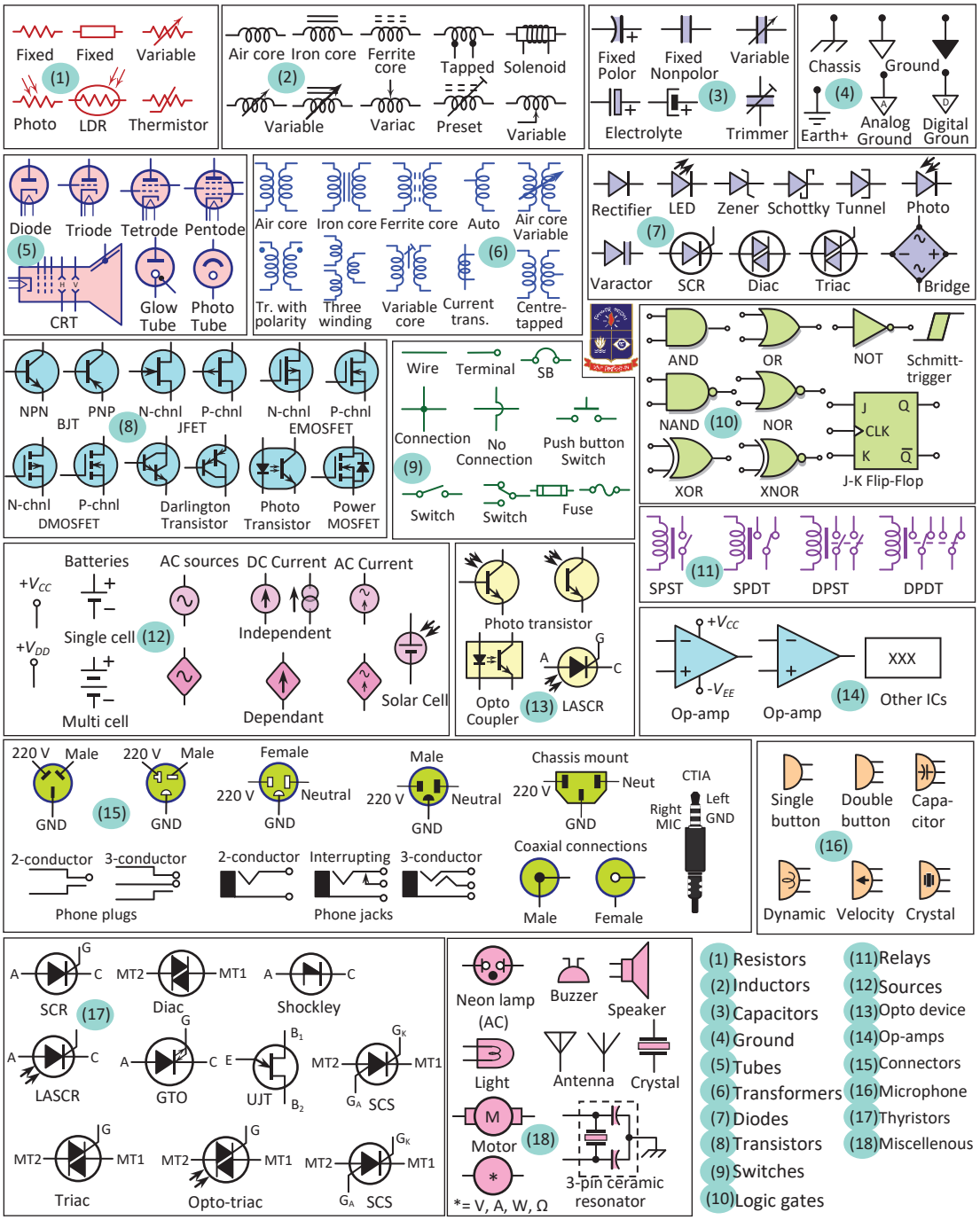


Fig.1-1: Symbols of some common components used in electronics

1.3 Electric Potential and Current

Any materials are made of atoms and atoms are made of electrons (negative charge), proton (positive charge) and neutron (chargeless). Normally, atoms possess equal number of electrons and protons. For this reason, any materials, like gold (Au), silver (Ag) copper (Cu), aluminum (Al) etc., have equal amount of positive charge and negative charge. As a result, normally each material is electrically neutral and has no potential difference. The situation is depicted in Fig.1-2 using water tank analogy. In Fig.1-2(a), there are two water tanks connected by a pipe.

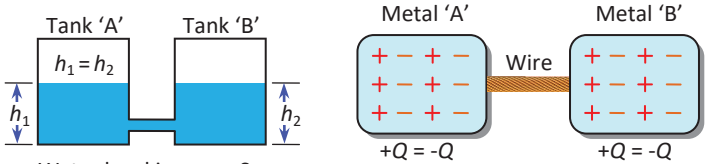


Fig.1-2: Concept of potential (a) Mechanical potential, and (b) Electrical potential

As the water levels are same in both the tanks, there is no potential (mechanical) difference, and hence, no flow of water. Similarly, in Fig.1-2(b), there are two metals, connected by a conducting wire. As the metals have equal number of positive and negative charges, so, there is no potential difference between them. Hence, there is no flow of charges or current.

But as shown in Fig.1-3(a), the water level in tank 'A' is higher than that in tank 'B'. So, there will have a mechanical potential difference, and hence, water will flow from tank 'A' to tank 'B' (higher potential to lower potential). Similarly, by any mechanism, if the positive charges and negative charges of metal 'A' and 'B' of Fig.1-3(b) are separated, there exists a potential difference. As shown in Fig.1-3(b), metal 'A' is at higher potential (higher positive charges) compared to metal 'B'. Therefore, positive charges will flow from metal 'A' to metal 'B' (actually electrons flow in opposite direction).

Potential difference tells us how much electrical energy is available to push electric charges through a circuit. The unit to measure electric potential difference is volt (V). Electric potential difference is also referred to as simply ***voltage***. Potential difference (or voltage) is measured by an instrument called ***Voltmeter***. It is always connected in parallel to the points where potential difference is to be measured as given in Fig.1-21(a).

As shown in Fig.1-3(a), due to the potential difference between tank 'A' and 'B',

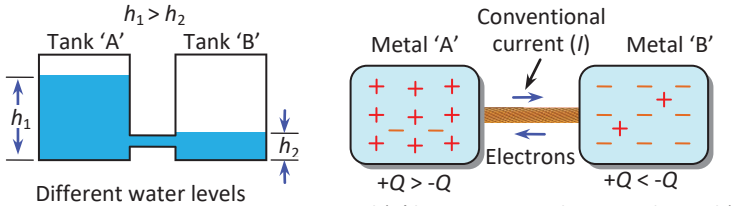
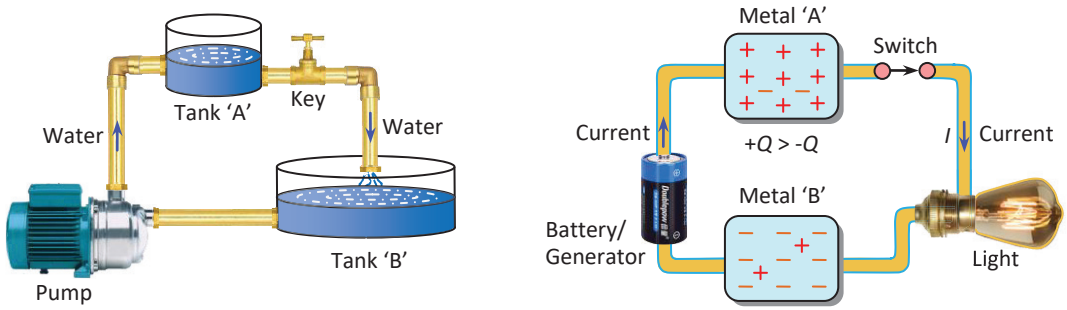


Fig.1-3: Concept of potential (a) Mechanical potential, and (b) Electrical potential

water will flow through the pipe connecting them. Similarly, due to the potential difference between metals 'A' and 'B', electric charge will flow from 'A' to 'B'. As positive charge cannot move, electrons will flow from metal 'B' to metal 'A' [Fig.1-3(b)]. The flow of charge will stop when the potential difference is zero. This flow of charge is called the ***current***. Actually the rate at which the electric charges flow through a device is called current. The unit used to measure the current is called ***Ampere*** (A). 1 ampere is equivalent to a flow of 1 Coulomb per second through the cross-section of a conductor or device. Although current was originally thought to be a flow of positive charge, we now know that in most cases it is the flow of electrons. The direction of conventional current is just opposite to the direction of electrons flow. The instrument used to measure the current is ***ammeter***. Unlike the voltmeter, ammeter is connected in series, so that, the full current can flow through the meter as shown in Fig.1-21(b).



(a) Continuous water flow using pump

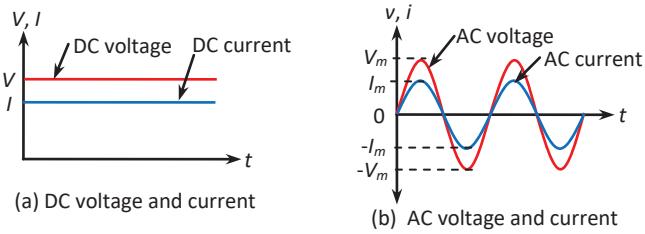
(b) Continuous current flow using battery or generator

Fig.1-4: Continuous flow of water and current with the help of external energy source

As shown in Fig.1-4(a), if we want continuous flow of water, we have to use a pump that will maintain the potential difference. Similarly, to get continuous current, we must use some source of electrical energy (battery or generator). The ***friction*** of the pipe that opposes the flow of water is analogous to the ***resistance*** in electrical circuit that opposes the flow of current.

1.4 AC and DC Currents

There are two types of voltage and current. These are: 1) ***DC voltage*** and ***current***, 2) ***AC voltage*** and ***current***. The examples of DC voltage sources are dry cell batteries, lead-acid batteries, DC power supply etc. The main property of these sources is that the voltage and current do not change with time (do not alternate). Fig.1-5(a) shows the graphs of DC voltage and DC current. The voltage produced by a generator is AC. The power coming from grid-line in our house is the example of AC voltage and current. The main property of these sources is that the voltage and current change with time (alternate). Fig.1-5(b) shows the graphs of AC voltage and AC current. The DC voltage and current is represented by their



(a) DC voltage and current

(b) AC voltage and current

Fig.1-5: AC and DC voltage and current

values only, whereas, the AC voltage and current are represented by their RMS (root-mean-square) values and frequency. In Bangladesh, the grid power used in households has 220 V (RMS) and 50 Hz.

1.5 Three Elements of Circuits (*RLC*)

A circuit is a complete path through which electric charge travels on. A simple circuit contains three components necessary to have electric activity, namely, ***sources of voltage***, ***conductive paths***, and ***resistors.*** In addition to resistors, electrical circuits may use two more components, these are ***capacitors*** and ***inductors***. A brief discussion on these elements is given here.

Resistors

Although any conducting wire of circuits produces unwanted resistance to the flow of current, we always add some resistance in circuits to control the current. The component that produces this resistance is called a ***resistor***. A resistor is a passive two-terminal electrical component that provides resistance (opposition) to the flow of charges. The ability of a resistor to resist the current is called ***resistance*** and is denoted by R.

In electronic circuits, resistors are used to reduce current flow, adjust signal levels, to divide voltages, and bias active elements (like diodes and transistors). Resistance of a conducting wire is given by

$$R = \rho \frac{l}{A} \tag{1-1}$$

where, ρ is the resistivity of the material of the wire, l is the length of the wire, and A is its cross-sectional area. Different materials have different values of ρ. Silver has the lowest value of ρ.

To construct circuits, resistors of different values and shapes are used. Different resistors have different resistance and power rating. Some of the resistors commercially available in the market are shown in Fig.1-6.

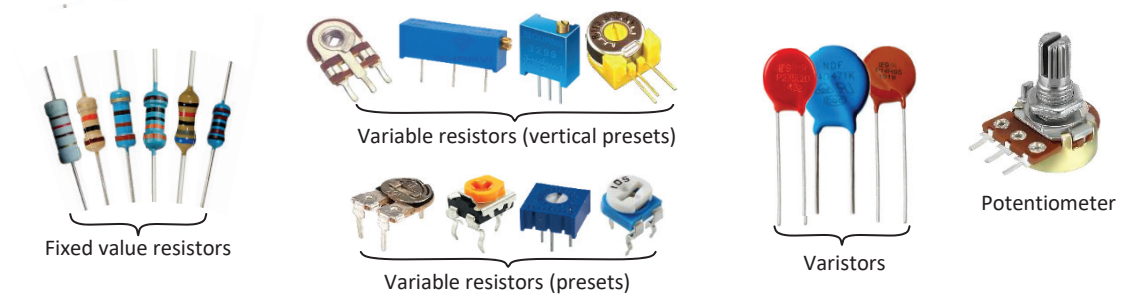


Fig.1-6: Photographs of different fixed and variable resistors

Color Code Marking of Leaded Resistors

The value of resistance of a resistor is written on it using different colors called ***color code***. The resistance color code consists of three or four color bands and is followed by a band representing the tolerance (variation of resistance). Another color is sometimes used

which is the temperature coefficient band. If provided, it is to the right of the tolerance band.

In the resistance color codes, the first two or three colors give the significant figures of the resistance value (in ohms), followed by a multiplier color. This is a factor by which the significant figure must be multiplied (i.e. the number of zeros to be added after the significant figures) to find the actual resistance value. The next color is the tolerance of the resistance. The tolerance of a resistor is the maximum difference between its actual value and the written value. For example, the actual value of a $1\text{k}\Omega \pm 20\%$ resistor may have any value between $800\ \Omega$ to $1200\ \Omega$. The color to the right of tolerance band (if any) is the temperature coefficient of resistance (TCR). TCR tells how much resistance changes as its temperature changes. It is usually expressed in $\text{ppm}/°\text{C}$ (parts per million per degree Celsius) units.

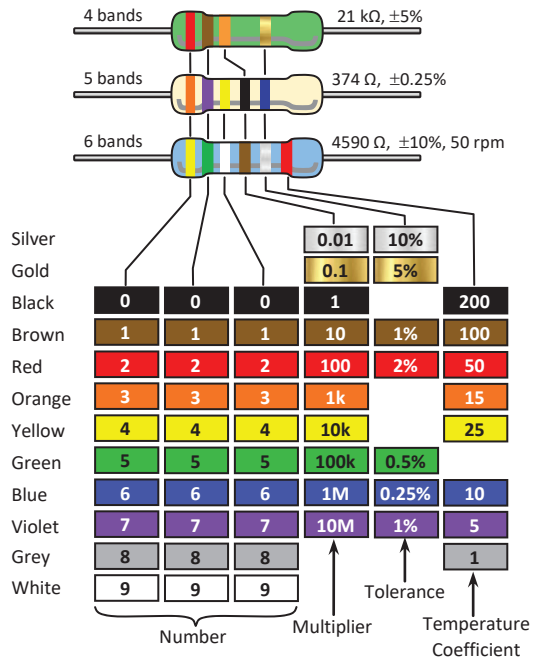


Fig.1-17: Process to read color codes of resistors

As shown in Fig.1-7, the colors on a resistor represent a number (decimal digit). We can remember these numbers using a popular sentence: "B B ROY Good Boy Very Good Worker" (Fig.1-8). First "B" is black and its value is "0" and the second "B" is brown = "1".

Fig.1-8.: Process to memorize values of colors

Example 1.1

Determine the resistance value of the resistor shown in Fig.1-9.

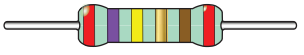


Fig.1-9: Resistor for Example 1.1

Solution:

Here, the first three colors are Red(2)-Violet(7)-Yellow(4). So the significant figure will be 274. The multiplier color is Gold=0.1, and the tolerance is Brown=1%. Therefore, the value of this resistor will be $274 \times 0.1 \pm 1\% = 27.4\ \Omega \pm 1\%$. Moreover, the Red color on the rightmost position represents $50\ \text{ppm}/°\text{C}$ TCR.

Comments: $50\ \text{ppm}/°\text{C}$ TCR means, its resistance will not change more than 0.00005 ohms (50/1,000,000) per ohm per degree Celsius temperature change (within the rated temperature range of -55 to +145°C, measured from 25°C room temperature.)

1.6 Capacitors and Capacitance

A capacitor (originally called condenser) is a passive two-terminal electrical component used to store electrostatic energy. Though the shapes and sizes of practical capacitors vary widely (Fig.1-14), but all capacitors contain two electrical conducting plates separated by a dielectric (i.e., insulator). The conductors can be thin films of metal, aluminum foil (rolled cylindrically) or disks, etc. (Fig.1-10 and 11). Capacitors are widely used as parts of electrical circuits in many common electrical devices. Unlike a resistor, a capacitor does not dissipate energy. Instead, a capacitor stores energy in the form of electrostatic field between its plates.

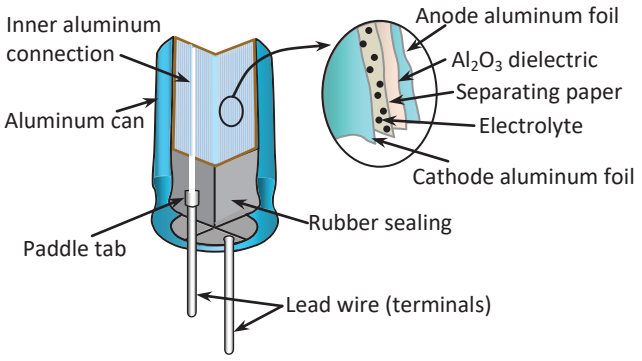


Fig.1-10: Construction of electrolytic capacitors

When potential difference is applied across a capacitor, negative charge accumulates on one palate and positive charge on the other plate as shown in Fig.1-11. Due to these opposite charges between the dielectric film, an electric field is developed. The ability of a capacitor to store charge is called ***capacitance*** and is denoted by *C*. The SI unit of capacitance is Farad (F), which is equal to one coulomb per volt (1 C/V). The capacitance of a capacitor will be $1\,\mathrm{F}$, if the capacitor can store 1 Coulomb charge for $1\,\mathrm{V}$ potential difference applied to its plates. Farad is a very large unit, so the practical unit of capacitance is microfarad ($1\mu\mathrm{F} = 10^{-6}\mathrm{F}$).

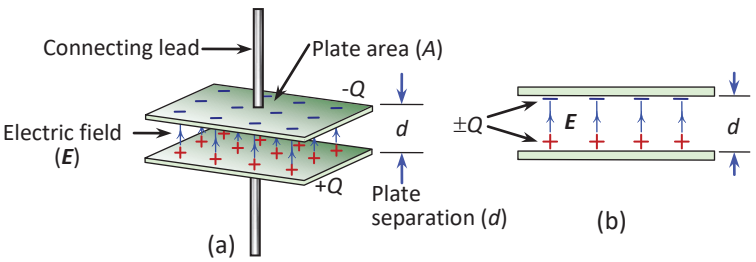


Fig.1-11: Components of a parallel plate capacitor with charge and field: (a) 3-D view, and (b) 2-D view

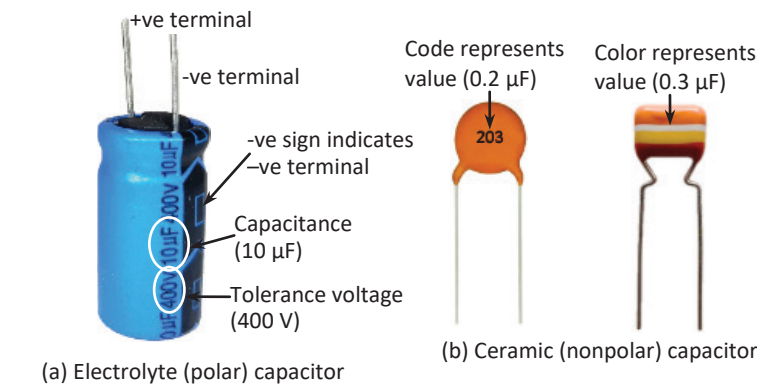


Fig.1-12: Values are written in different ways on capacitors

In practice, the dielectric between the plates has an electric field strength limit, known as the ***breakdown voltage***. This voltage is called the ***tolerance voltage*** of the capacitor. In some

capacitors (e.g. electrolytic capacitors), the tolerance voltage is written on the capacitor [Fig.1-12(a)]. The applied voltage to a capacitor must be equal or less than the tolerance voltage.

In non-polar capacitors (ceramic, miller, tantalum etc.) the value of the capacitance is either written as a code number (Fig.1-12) or using colors. In coding system, the first 2 digits give the value and the 3rd digit is the multiplier, that is used as a power of 10 and the value will be in pico-Farad (pF). For example, the code number written on a ceramic capacitor is 203 [Fig.1-12(b)]. Its value will be 20×10^3 pF $= 20000$ pF $= 0.02$ μF or 20 nF.

Capacitors are widely used in electronic circuits for blocking direct current while allowing alternating current to pass. In analog filter networks, they smooth the output of power supplies. In resonant circuits they tune radios to particular frequencies. In electric power transmission systems they stabilize voltage and power flow.

Already we have discussed that a capacitor can store charge. In DC (direct current) circuits capacitors store charges, but in AC circuits capacitors work just like a resistor. The opposition produced by a capacitor to the AC current is called ***capacitive reactance*** and is denoted by X_C. The reactance of a capacitor is inversely proportional to its capacitance and the frequency of the AC current. Mathematically,

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \qquad (1\text{-}2)$$

where, f is the frequency of AC current and C is the capacitance of the capacitor.

For AC voltage, the capacitor behaves as a linear device, i.e., if the frequency and the capacitance are constant, the capacitor current will increase linearly with the increase in AC voltage.

Example 1-2

Determine the value of capacitance of the capacitor shown in Fig.1-13. Calculate the value of reactance (X_C) if the capacitor is used for 50 Hz AC voltage.

Fig.1-13: Ceramic capacitor for Example 1-2

Solution:

The code number written on the capacitor is 104. So, the value of capacitance will be 10×10^4 pF $= 100000$ pF $= 0.1$ μF or 100 nF. The reactance can be calculated using Equ.(1-2).

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(50\text{ Hz})(0.1 \times 10^{-6})} \approx 32\text{ k}\Omega\text{ [Ans.]}$$

Comments: In Bangladesh, the frequency of AC supply voltage is 50 Hz. Hence, here we have considered $f = 50$ Hz.

The shapes and sizes of practical capacitors vary widely according to their applications. A number of capacitors are available in markets. Some of the common capacitors are shown in Fig.1-14.

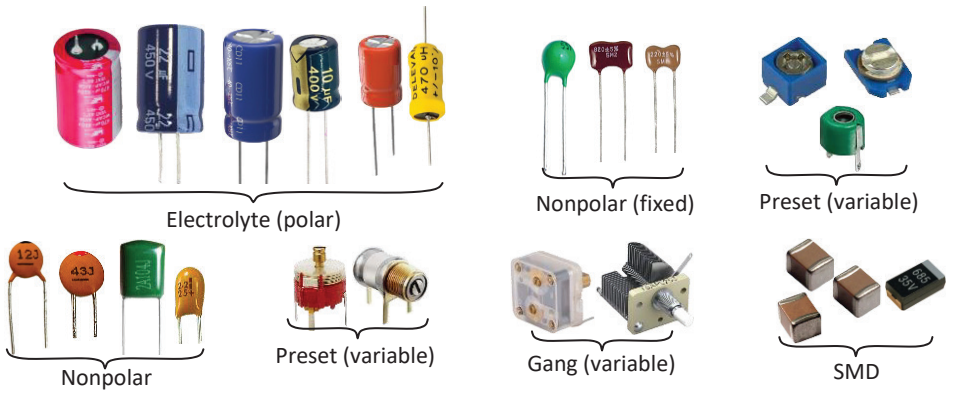


Fig.1-14: Photographs of various fixed value and variable capacitors available in market

1.7 Inductors

Inductor (also called coil, choke, or reactor) is a passive two-terminal electrical component that stores energy in magnetic field when electric current flows through them. An inductor typically consists of an insulated wire, wound into a coil around a core (Fig.1-15). When current flows through an inductor magnetic field is produced inside the coil as shown in Fig.1-16(a). If the current flowing through the inductor changes with time, magnetic field also varies with time, and this time-varying magnetic field induces an electromotive force or voltage ($\epsilon = -Ndi/dt$) across the inductor as described by Faraday's law of electromagnetic induction [Fig.1-16(c)]. According to Lenz's law, the induced voltage has such a polarity (direction) that it opposes the change in current that produces it. As a result, inductors oppose any change in current (AC current) through them by inducing a voltage (in opposite direction). The ability of an inductor to oppose the AC current is measured by a parameter called ***inductance*** and is denoted by L. Inductance is defined as the ratio of the induced voltage to the rate of change of current ($L = e/(di/dt)$. In the SI system, the unit of inductance is ***Henry*** (H). Along with capacitor and resistor, inductor is one of the three passive linear circuit elements that make up electrical and electronic circuits.

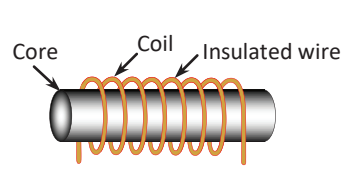


Fig.1-15: Inductor

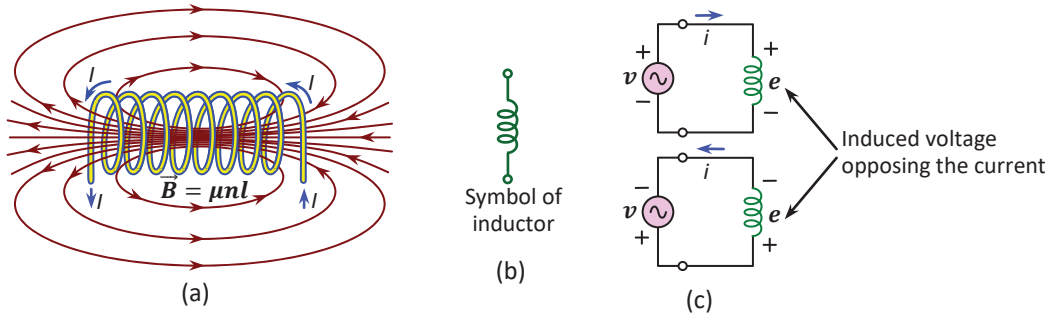


Fig.1-16: Inductor: (a) Coil with magnetic field, (b) Symbol of inductor, and (c) Inductors with induced voltage

Inductors are widely used in alternating current (AC), electronic equipment, particularly in radio equipment. They are used to block AC while allowing DC to pass. Unlike the capacitors, inductors oppose the AC current flowing through them. The opposing parameter of an inductor to AC current is called ***inductive reactance*** (X_L) and is given by,

$$X_L = \omega L = 2\pi f L \qquad (1\text{-}3)$$

The value of inductance is written directly on the device or using color code. Although, there is variation in number of colors, a 4-band color code system is shown in Fig.1-17.

There are various types of inductors available in the market with different values, sizes and shapes. To be familiar with them, photographs of some common inductors are given in Fig.1-18.

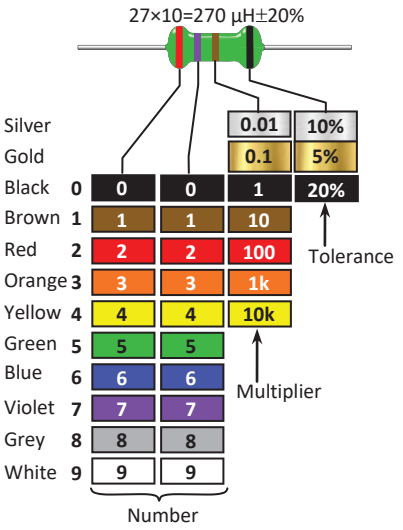


Fig.1-17: Process to read color codes of inductor

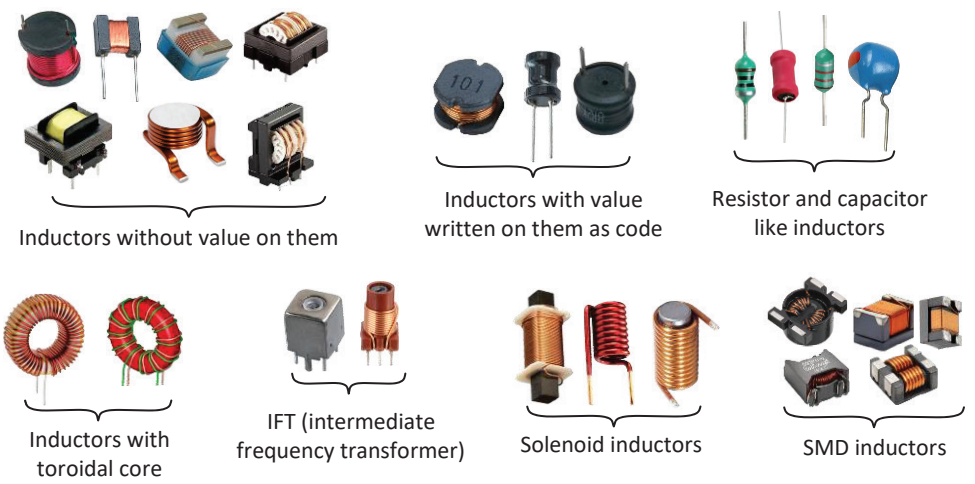


Fig.1-18: Photographs of various inductors available in market

1.8 Use of Multimeter

A ***multimeter*** is an electronic (or electrical) instrument that is used to measure voltage, current, resistance etc. Actually a multimeter is a combination of ***voltmeter***, ***ammeter***, ***and ohmmeter*** and so on. Being a versatile instrument, it is most commonly used for measuring different components (resistors, inductors, capacitors, diodes, transistors etc.) and parameters (voltage, current, power etc.) of electronic (and electrical) circuits. It is also used for continuity testing

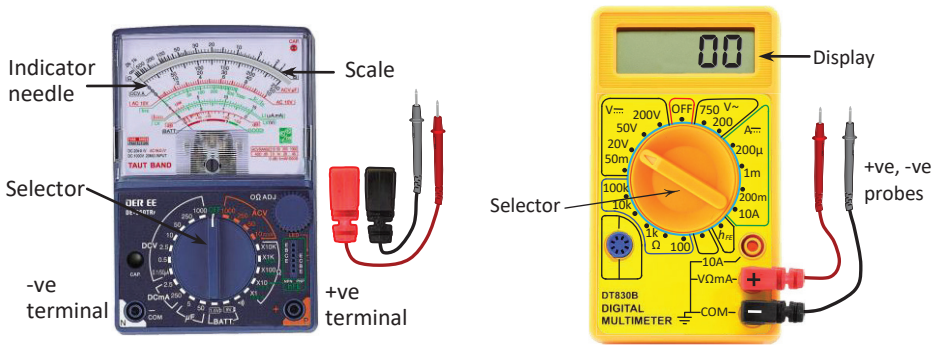


Fig.1-19: Analog and digital multimeters

purpose in servicing electrical and electronic circuits. There are mainly two types of multimeters: (1) ***Analog multimeter***, and (2) ***Digital multimeter***. The photographs of an analog and a digital multimeter are shown in Fig.1-19.

The main difference between them is, the analog multimeter has an indicating needle that moves on a scale to indicate the value of the measured parameter. On the other hand, the digital multimeter has a display unit, that directly shows the value (numerically) of the measured parameter. Both multimeters have a selector that has to be set to appropriate position (type of parameter and values) before using. We have to be careful to use these meters. The selector has to be set such a range that is greater than the value to be measured. For example if we want to measure line voltage using digital multimeter, the selector has to be set in the voltage range 750 V AC. Fig.1-20 shows how to measure the supply voltage in our house using a digital multimeter. As there is risk of shock, we must not touch the metallic portion of the meter probes.

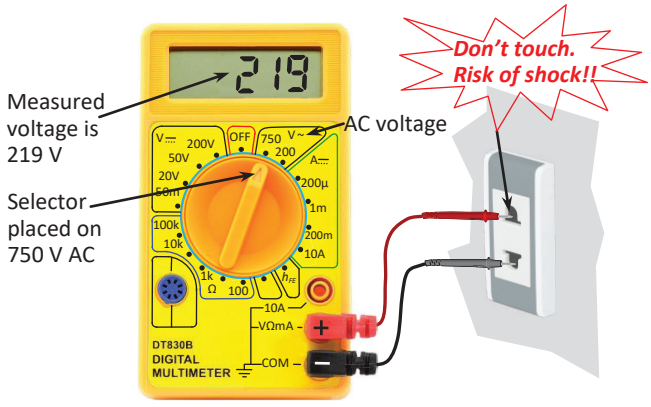
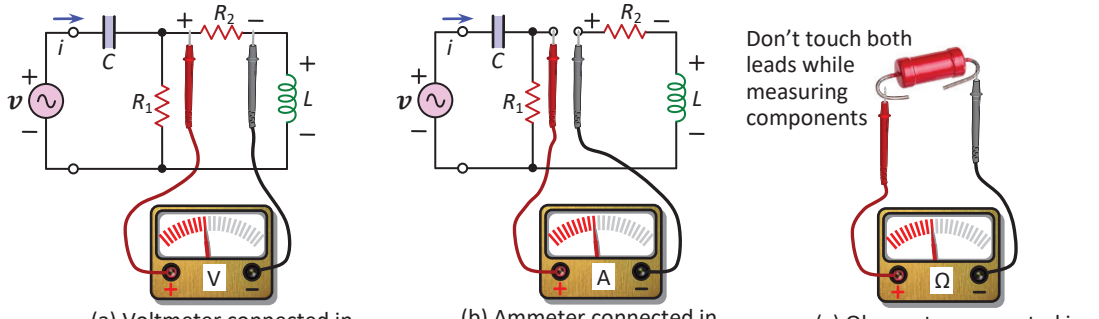


Fig.1-20: Digital multimeter measuring line voltage

Measuring process of different parameters and elements are shown in Fig.1-21. To measure voltage the voltmeter has to be connected across two points or across the components [Fig.1-21(a)]. To measure current the meter has to be connected in series, that is, the current measuring point has to be opened and then connect the ammeter [Fig.1-21(b)]. Moreover, to measure resistance, capacitance, inductance etc. the meter has to be connected in parallel to those components [as shown in Fig.1-21(c)]. As human body has a finite resistance, we should not hold the components' both terminals by hand (holding one terminal is OK) while measuring

these components. If we hold both terminals, our body resistance will work in parallel to the measured components, so the reading may not be accurate.



(a) Voltmeter connected in parallel

(b) Ammeter connected in series

(c) Ohmmeter connected in parallel with the components

Fig.1-21: Meter connection methods: (a) Voltage measurement, (b) Current measurement, and (c) Components measurement

1.9 Different Laws used in Electronics

Ohm's Law

Ohm's law gives the relationship between electric current and potential difference. The current that flows through a conductor (or resistor) is directly proportional to the potential difference (voltage) applied to it. Georg Simon Ohm, a German physicist was the first to state this law.

Ohm expressed his discovery in the form of a simple equation, describing how voltage, current, and resistance are interrelated:

Ohm's law equation

$$V = IR \tag{1-4}$$

In this algebraic expression, voltage (V) is equal to current (I) multiplied by resistance (R). Using algebra, we can manipulate this equation into two other variations to measure current (I) and resistance (R) as:

$$I = V/R \tag{1-5}$$

$$R = V/I \tag{1-6}$$

Using these equations we can calculate the value of any one parameter if the other two are known.

Let's see how these equations are used to analyze simple circuits.

In the circuit of Fig.1-22, there is only one source of voltage (the battery) and only one source of resistance (R) to current. The value of current can easily be calculated using Ohm's Law. Let the applied voltage be 12 V and the resistance be 200 Ω. Therefore, the current flowing through this circuit will be,

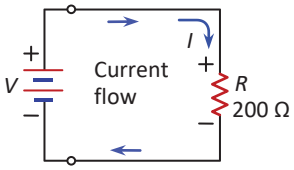


Fig.1-22: Ohm's law applied to a simple circuit

$$I = \frac{V}{R} = \frac{12\ \text{V}}{200\ \Omega} = 0.06\ \text{A} = 60\ \text{mA}$$

If we know the values of *V*, and *I* we can determine the value of the resistance as

$$R = \frac{V}{I} = \frac{12\ \text{V}}{60\ \text{mA}} = \frac{12\ \text{V}}{60\ \text{mA} \times 10^{-3}} = 200\ \Omega$$

If we know the values of *I*, and *R*, we can determine the voltage of the battery as,

$V = IR = 60\ \text{mA} \times 10^{-3} \times 200\ \Omega = 12\ \text{V}.$

Kirchhoff's Laws

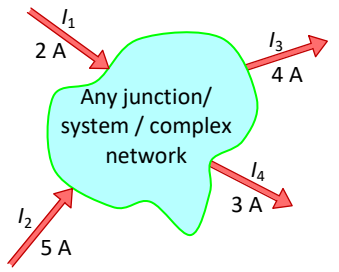


Fig.1-23: KCL applied to a simple circuit

Kirchhoff's laws quantify how current flows through a circuit and how voltage varies around a loop in a circuit. ***Kirchhoff's current law*** (**KCL**) states that the algebraic sum of the currents entering and leaving an area, system, or junction is zero. In other words, the sum of the currents entering an area, system, or junction must equal the sum of the currents leaving the area, system, or junction.

In Fig.1-23, for instance, the shaded area can enclose an entire system, a complex network, or simply a junction of two or more electrical paths. In each case, the current entering must equal the current leaving. That is,

$$I_1 + I_2 + (-I_3) + (-I_4) = 0$$

or, $$I_1 + I_2 = I_3 + I_4$$

or, $$2\ \text{A} + 5\ \text{A} = 4\ \text{A} + 3\ \text{A}$$

Kirchhoff's voltage law (**KVL**) states that the algebraic sum of the potential rises and drops around a closed loop (or path) is zero. A closed loop is any continuous electrical path that leaves a point in one direction and returns to that same point from another direction without leaving the circuit. In Fig.1-24, by following the current, we can trace a continuous path that leaves point 'A' through R_2 and returns to the same point through *E* without leaving the circuit. Therefore, ABCDA is a closed loop or path. We can apply KVL considering the loop in clockwise direction or counterclockwise direction. The result will be exactly same. To apply KVL properly, we must know the polarities of voltage drops. The terminal of a resistor into which the conventional current enter will be positive (+) and the terminal from where the conventional current leaves will be negative (-). '+' means higher potential and '-' means lower potential. So, there must have a potential difference across the resistor (between '+' and '-' sign). In applying KVL around a loop, if we move from '+' to '-', the potential difference will be negative, and if we move from '-' to '+', the potential difference will be positive.

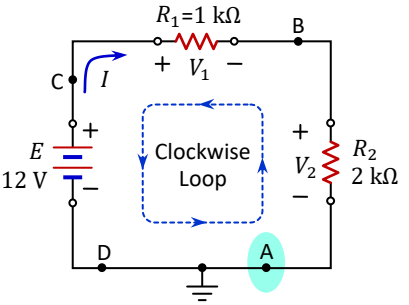


Fig.1-24: KVL applied to a simple circuit

So, applying KVL in the loop of Fig.1-24, we can write,

$$+V_2 + V_1 - E = 0$$

Or using Ohm's law, $$+IR_2 + IR_1 - E = 0$$

Voltage Divider Rule

Voltage divider rule is a method by which a voltage in a series circuit can be determined without calculating the current in the circuit. The voltage divider rule states that the voltage across a resistor in a series circuit is equal to the value of that resistor times the total applied voltage across the series elements divided by the sum of the series resistances.

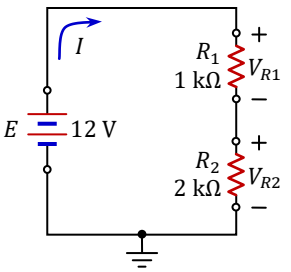


Fig.1-25: Voltage divider rule applied to a simple circuit

Applying voltage divider rule we can easily calculate the voltage across the resistors of Fig.1-25 as,

$$V_{R1} = E \times \frac{R_1}{R_1 + R_2} = 12\text{ V} \times \frac{1\text{ k}}{1\text{ k} + 2\text{ k}} = 4\text{ V}$$

and, $$V_{R2} = E \times \frac{R_2}{R_1 + R_2} = 12\text{ V} \times \frac{2\text{ k}}{1\text{ k} + 2\text{ k}} = 8\text{ V}$$

The Current Divider Rule

Current divider rule is used in parallel circuits (or elements). For parallel elements of different values, the current will split with a ratio equal to the inverse of their resistance values.

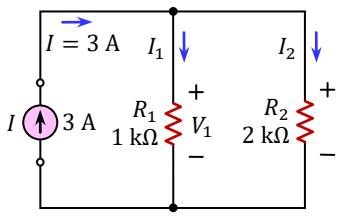


Fig.1-26: Current divider rule applied to a simple circuit

For the parallel resistors of Fig.1-26, the current flowing through the resistors (R_1 and R_2) can be calculated using current divider rule as,

$$I_1 = I \times \frac{R_2}{R_1 + R_2} = 3\text{ A} \times \frac{2\text{ k}}{1\text{ k} + 2\text{ k}} = 2\text{ A}$$

and, $$I_2 = I \times \frac{R_1}{R_1 + R_2} = 3\text{ A} \times \frac{1\text{ k}}{1\text{ k} + 2\text{ k}} = 1\text{ A}$$

Note: The laws and the rules, discussed so far, are also applicable for AC voltage. For circuits constructed using only resistors, the laws and the rules can be directly used as described above. However, if the circuit contains capacitor and/or inductor then we have to use the reactances of these components. Moreover, there will have a phase difference between the voltage and current due to the effect of capacitors and inductors.

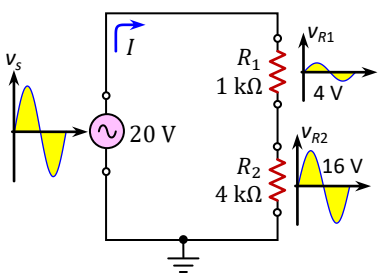


Fig.1-27: Voltage divider rule used for AC voltage

Fig.1-27 shows the use of voltage divider rule for AC voltage. Here, 20 V (p-p) AC supply has been proportionately divided across the resistors R_1 and R_2 according to the voltage divider rule.

CHAPTER

2

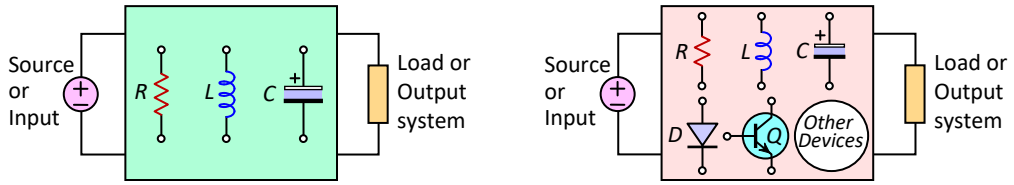
PN Junction Diodes

2.1 Introduction

In ***Basic Electronics*** course, various types of devices and circuits are discussed. In the past, electronic circuits were constructed using vacuum tubes. The simplest vacuum tube, the diode, was invented in 1904. In 1947, Bardeen and Brattain at Bell Laboratories in the US invented the point-contact transistor, and in 1948 Shockley invented the junction transistor. Since then, new semiconductor devices have been invented and used in constructing electronic circuits. Already we know that a complete conducting path of charge flow is called a circuit. There are two types of circuits - electrical circuits and electronic circuits.

Electrical Circuits: An ***electrical circuit*** is a complete path in which, charge (i.e. electrons) flows from a voltage or current source. This type of circuit consists of three elements – resistors, capacitors and inductors but no semiconductor device or vacuum tube (Fig.2-1). They have no processing capability of signals.

Electronic Circuits: An electronic circuit is also a complete path in which charge (i.e. electrons) flows from a voltage or current source, but here, they have processing capability of signals. That is, electronic circuits can amplify, rectify or attenuate a signal and so on. Electronic circuits are also consisting of resistor, capacitor and inductor, but they must have at least one vacuum tube or semiconductor device- like a diode, a transistor etc.



(a) Electrical circuit (b) Electronic circuit

Fig.2-1: Electrical and Electronic circuits

2.2 Insulator Conductor and Semiconductor

In any materials the maximum energy of an electron may be that of the valence electrons. That is, electrons can exist at most in the valence band (outermost bands). The difference between the conduction band (energy band of free electrons) and the valence band is called ***Energy gap*** (E_g). Current carrying capacity of a material depends on the value of E_g. Depending on the current carrying capacity materials are divided into three categories as described below.

Insulators

The materials that cannot carry electricity (flow of charge) are called ***insulators***. The energy gaps (E_g) of these materials are very high so no electrons can get sufficient energy from external sources to go to the conduction band [Fig.2-2(a)]. Generally, the values of E_g of insulators are greater than 5 eV (electron-volt). Examples of insulators are rubbers, plastic, wood, cloths etc. Rubbers and plastics are used as insulating cover of electrical wire.

Conductors

The materials that can carry electrical current easily are called ***conductors***. In these materials, there is no energy gap between the conduction band and the valence band. In fact, there is an overlap between the conduction band and the valence band [Fig.2-2(b)]. For the overlap of the bands, some electrons of the valence band also possess the energy of the conduction band. These electrons behave as free electrons and can carry electrical current easily. Examples of conductors are silver, gold, copper, aluminum etc. The conductivity order of some common materials are: silver (Ag) > copper (Cu) > gold (Au) > aluminum (Al) > zinc (Zn) > nickel (Ni) > brass > bronze > iron (Fe).

Semiconductor

In between conductors and insulators, there are some materials called ***semiconductors***. They are neither good conductor nor insulator. The materials with $E_g < 5$ eV are called semiconductors [Fig.2-2(c)]. At absolute zero temperature, the conduction bands of these materials are completely empty, i.e., they have no free electrons. But at room temperature, some electrons of valence band can gain sufficient energy to jump to the conduction band. Thus, at room temperature they can carry electricity, but their resistivity is high compared to that of conductors. Examples of semiconductors are: silicon (Si), germanium (Ge), boron (B), phosphorus (P) etc. At room temperature, the values of energy gaps of some common semiconductors are given in Fig.2-2(c).

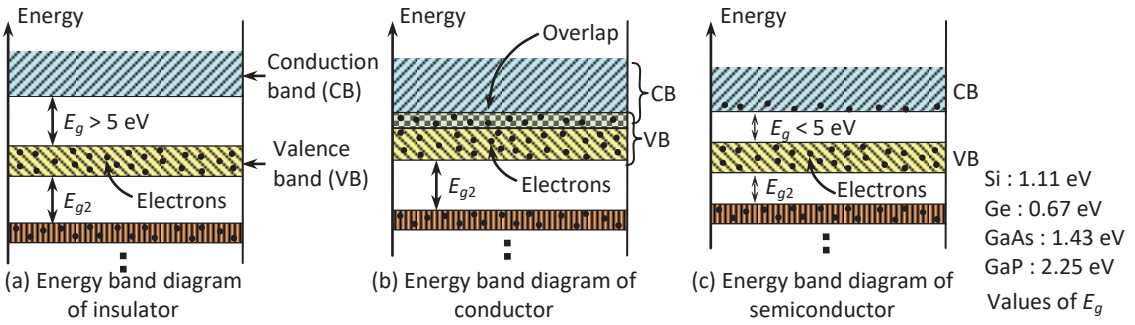


Fig.2-2: Energy band diagrams of different materials

Semiconductor materials are divided into two categories. These are ***intrinsic*** semiconductor and ***extrinsic*** semiconductor.

2.3 Intrinsic Semiconductor

Semiconductor in its purest form is called ***intrinsic*** semiconductor. Semiconductors used for different purpose have different purity levels. Metallurgical-grade semiconductor has the purity level of 98-99%, whereas the purity level of electronic-grade semiconductor is as high as 99.9999%. At room temperature some electrons can absorb sufficient amount of thermal energy to move to the conduction band leaving behind a vacancies of electrons in the valence band which are called ***holes***. So, an intrinsic semiconductor has some free electrons in the conduction band and an equal number of holes in the valence band. At room temperature (300 K), the intrinsic carrier concentration (electrons, n_i and holes p_i) per cubic centimeter is 1.5×10^{10} for silicon, 2.4×10^{13} for germanium and 2.1×10^{6} for gallium-arsenide. On the other hand, Cu contains 8.4×10^{22} free charge carriers (electrons) per cubic centimeter. For intrinsic semiconductor $n_i = p_i$.

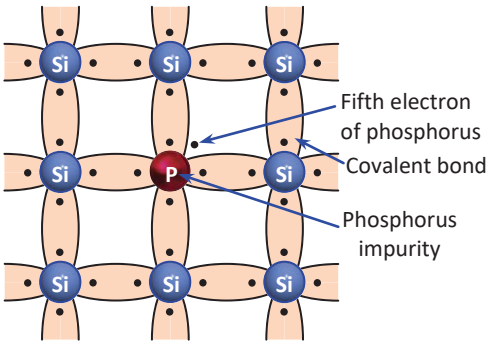
2.4 Extrinsic semiconductor

A semiconductor when mixed with some impurity is called ***extrinsic*** semiconductor. The process of mixing impurity is called ***doping*** and the impurity itself is called ***dopant*** atom. The order of mixed impurity is 1 to 100 ppm (part per million). These mixed impurity atoms produce some additional energy levels in the energy gap of the semiconductor and hence decrease the energy gap. Now, at room temperature, more electrons can go to the conduction band from the added impurity bands. Thus the conductivity of the extrinsic semiconductor increases. Extrinsic semiconductors are of two types- ***N-type semiconductor*** and ***P-type semiconductor***.

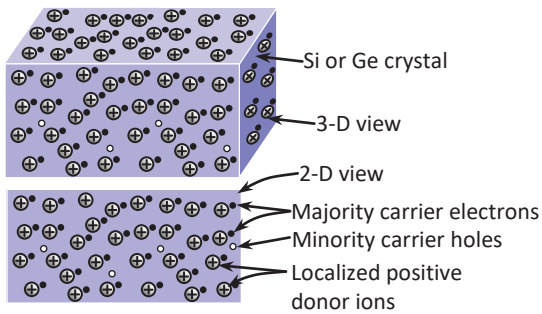
N-type or Negative-type Semiconductor

Both the N-type and P-type semiconductor materials are formed by adding suitable impurity atoms into a pure semiconductor (Si, Ge, etc.). The N-type semiconductor is created by introducing elements that have five valence electrons (pentavalent elements), such as phosphorus, arsenic, antimony etc. The effect of the added impurity elements (phosphorus in silicon crystal) is depicted in Fig.2-3(a). There are five valence electrons at the outer most shell of phosphorus atoms. But four valence electrons form four covalent bonds with four adjacent silicon atoms. The fifth electron of

phosphorus atom remains unused. Every phosphorus atom added to the Si crystal has such an unused electron. These electrons are loosely bound to the parent atoms and can jump to the conduction band at room temperature and behave as ***free electrons***. In this way, by adding suitable amount of pentavalent impurity atoms, the number of free electrons can be increased to a desired level. Now, as the crystal has many free electrons (negative charge), it is called ***N-type semiconductor*** (N for negative). The impurities with five valence electrons are called ***donor atoms***.



(a) Effect of adding phosphorous in Si crystal



(b) 3-D and 2-D view of N-type semiconductors

Fig.2-3: Preparation of N-type semiconductor doping with pentavalent impurities

Note that a discrete energy level, called the ***donor level*** (E_{gd}) is developed closed to the conduction band. E_{gd} (energy gap of donor level) is significantly less than that of the intrinsic material (E_g) as shown in Fig.2-3(c). Those unused electrons of the added impurity atoms can absorb sufficient thermal energy to move into the conduction band at room temperature. The result is that at room temperature, there are a large number of charge carriers (electrons) in the conduction band. So, the conductivity of the material increases significantly. Although, electrons are the majority charge carriers in N-type semiconductor, at room temperature some electrons move from the valence band to the conduction band and produce some holes in the valence band. These holes are called minority carries in N-type semiconductor.

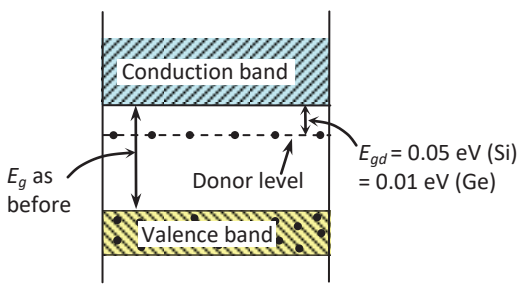
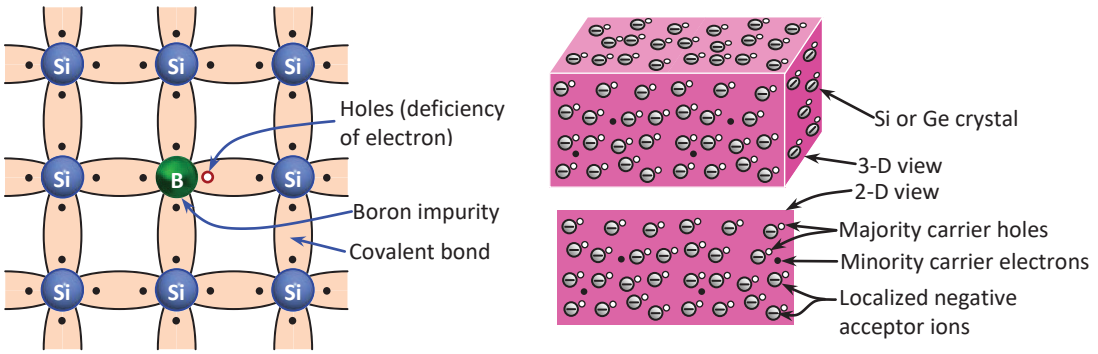


Fig.2-3(c) Energy band diagram of N-type semiconductor

In summary, we can say, an N-type semiconductor has electrons as majority carriers, and holes as minority carriers as shown in Fig.2-3(b). As every donor atom donates one electron, electrically it becomes positive. They cannot move and remain as ***localized positive ions*** in the crystal.

P-type or Positive-type Semiconductor

The P-type semiconductor material is developed in the same process. A pure germanium or silicon crystal is doped with impurity atoms having three valence electrons (i.e., trivalent impurities). Examples of such impurities are: boron (B), gallium (Ga), and indium (In) etc.



(a) Effect of adding boron in Si crystal

(b) 3-d and 2-d view of P-type semiconductors

Fig.2-4: Preparation of P-type semiconductor doping with trivalent impurities

The effect of adding boron atoms in silicon is indicated in Fig.2-4(a). Three electrons of the outer most shell of boron form three covalent bonds with three adjacent Si atoms. But the fourth adjacent Si atom cannot form a complete covalent bond due to an electron deficiency. This deficiency of electron is called a ***hole*** and is represented by a circle or a plus sign. The holes behave like positive charge because they can capture electrons. Since, the trivalent impurities capture (accept) electrons, they are called ***acceptor***. Every acceptor added in the silicon crystal introduces an energy state in the energy band diagram. This energy level is called ***acceptor level***. The acceptor level is produced in between the conduction band and the valence band, close to the valence band [Fig.2-4(c)]. The energy difference between the valence band and the acceptor level (E_{ga}) is very small. At room temperature, electrons can easily absorb sufficient heat energy and jump from the valence band to the acceptor level. The electrons that move to the acceptor level, leave behind holes in the valence band. Thus many holes are developed in the valence band. The holes are the majority charge carriers in P-type semiconductor. As in the case of intrinsic semiconductors, some electrons will absorb sufficient thermal energy and will jump from valence band to the conduction band. These electrons are called minority charge carriers.

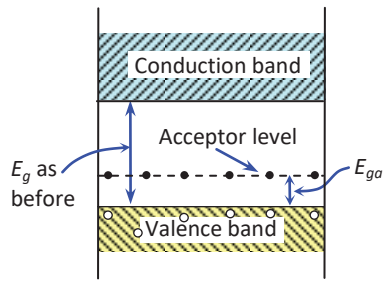


Fig.2-4(c): Energy band diagram of P-type semiconductor

In summary, we can say, a P-type semiconductor has holes as majority carriers, electrons as minority carriers and negatively charged localized acceptor ions as shown in Fig.2-4(b).

2.5 PN Junction Diode

If one half of a semiconductor slab is made P-type and the other half is made N-type or some portion of a semiconductor is made P-type and the rest of it is made N-type, a PN junction will be developed (Fig.2-5). Some changes take place at the interface of P-type and N-type material and a depletion layer and a barrier voltage (V_B) is developed.

As shown in Fig.2-5 there are majority of holes in the P-type semiconductor and majority of electrons in the N-type semiconductor. Due to this concentration variation electrons diffuse from N-type to P-type and holes diffuse to N-type. If an electron comes to P-type material it will neutralize a hole, similarly if a hole moves to N-type it will neutralize an electron. In this way, a region will be developed that has no free carrier as shown in Fig.2-6. This region, at the interface of P-type and N-type materials, is called ***depletion region*** or ***depletion layer*** as the region has been depleted off free charge carriers.

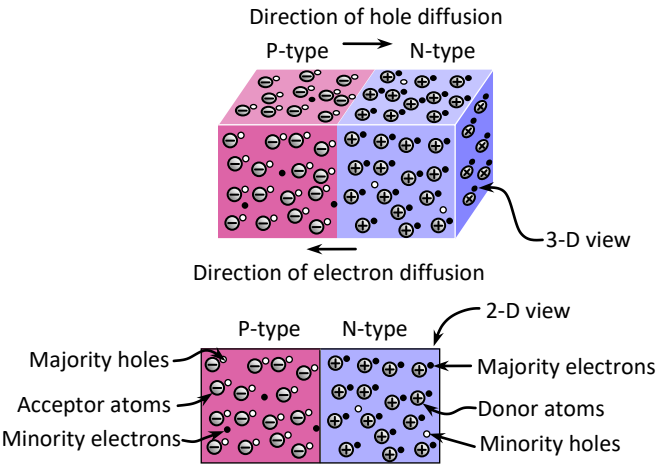


Fig.2-5: PN-junction before equilibrium

Note that there are localized acceptor ions in the depletion layer of P-type and donor ions in the N-type material. Since, acceptor ions are negative and the donor ions are positive, an ***electric field*** will be developed in the depletion layer and its direction will be from positive to negative, i.e., from N-type to P-type as shown in Fig.2-6. The direction of the electric field will be such that it will oppose the diffusion of majority carriers. With the diffusion of more and more majority carriers, the strength of the electric field will gradually increase. At a certain value of electric field strength the diffusion of the majority carriers will stop and we say that the PN junction has reached to ***equilibrium***. In other way, we can say that, the negative ions in the P-type and the positive ions in the N-type will produce a potential difference. Actually this potential difference will produce the aforesaid electric field. As this potential difference opposes the flow of majority carriers, it is called ***barrier voltage V_B***. For silicon PN junction, the typical value of the barrier voltage is ≈ 0.7 V and for germanium PN junction its value is ≈ 0.3 V.

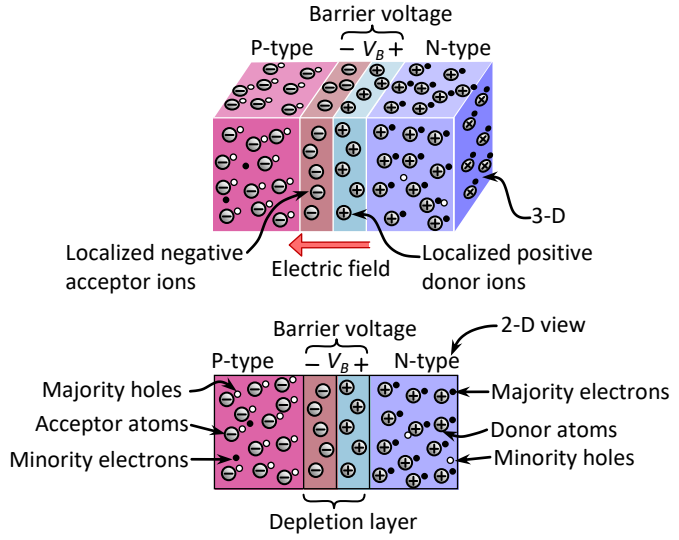


Fig.2-6: PN-junction at equilibrium (Barrier voltage and depletion layer formed by diffusion of carriers)

When metal contacts are made to the P-type and N-type semiconductor, as shown in Fig.2-7, a **PN *junction diode*** or simply a semiconductor ***diode*** is produced. The electrical symbol of a diode is shown in the same figure. The terminal connected to P-type material is called ***anode*** and that connected to N-type material terminal is called ***cathode***. The arrow head indicates the direction of the conventional current flow as will be described later.

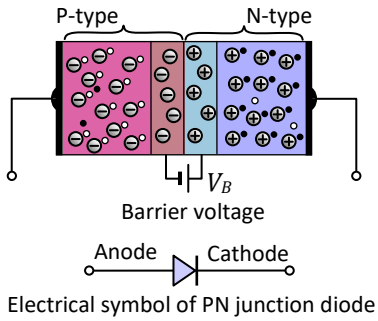


Fig.2-7: PN junction diode

2.6 Current in PN Junction at Equilibrium

When the barrier voltage V_B of a PN junction becomes 0.7 V (for Si) or 0.3 V (for Ge) the diffusion of majority carriers stops and the junction comes to an electrical equilibrium condition. However, at room temperature, both the majority and minority carriers produce random motions. Hence, if a minority carrier electron of P-type semiconductor comes within the depletion region (where the electric field exists), the electric field will push it to the N-side, called ***drift current***. Similarly, the minority carriers of N-type material drift to the P-side. In this way, two drift currents will be produced (Fig.2-8). The two drift currents will add up and will produce a resultant ***drift current*** as shown in the figure.

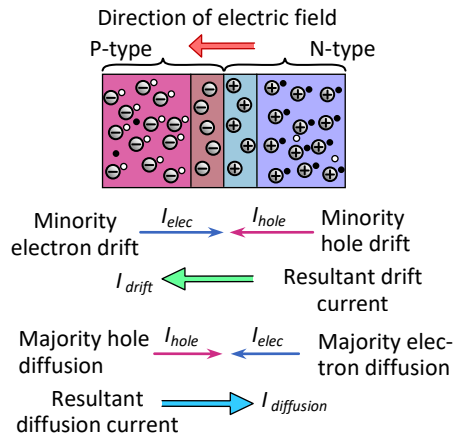


Fig.2-8: Current components of PN junction at equilibrium

As, due to the drift of minority carriers, the number of majority carriers has increased (both in P-side and N-side) than that without drift, hence, majority carrier hole will diffuse from P-type material to the N-type material and the majority carrier electrons will diffuse from N-type to P-type material. The two diffusion currents will also add up and will produce a resultant current which is called ***diffusion current***. As shown in Fig.2-8, at equilibrium condition, the magnitudes of the drift current and the diffusion current will be same, and the net resultant current through the PN-junction will be zero at equilibrium.

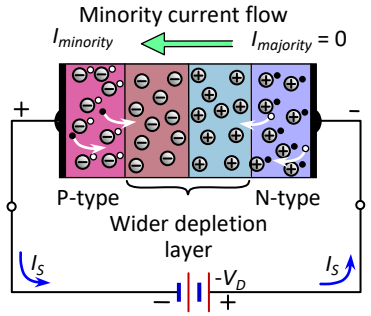
2.7 *I-V* Characteristic of a PN Junction Diode

Biasing is the process of applying an external potential (voltage) to a device. The voltage applied for biasing is called ***bias voltage***. A PN junction can be biased in forward direction or in reverse direction.

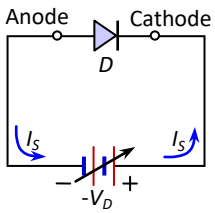
Characteristics in Reverse Biased Condition

When an external potential (i.e., a battery) is connected across a PN junction diode with the positive terminal of the battery connected to the N-type material and the negative terminal connected to the P-type material as shown in Fig.2-9, the situation is called ***reverse bias***. The

number of positive ions in N-type material of the depletion region will increase due to the large number of free electrons drawn by the positive terminal of the applied potential. For similar reasons, the number of negative ions will increase in the P-type material. The net effect, therefore, is that the width of the depletion region will increase. This widening of the depletion region will establish a greater barrier for the majority carriers reducing the majority carrier flow. The drift of the minority carriers, however, will continue. This results in a very small current from N-side to P-side.



(a) Circuit using constructional blocks of PN junction



(a) Circuit using schematic symbol of PN junction

Fig.2-9: Reverse biased PN junction diode

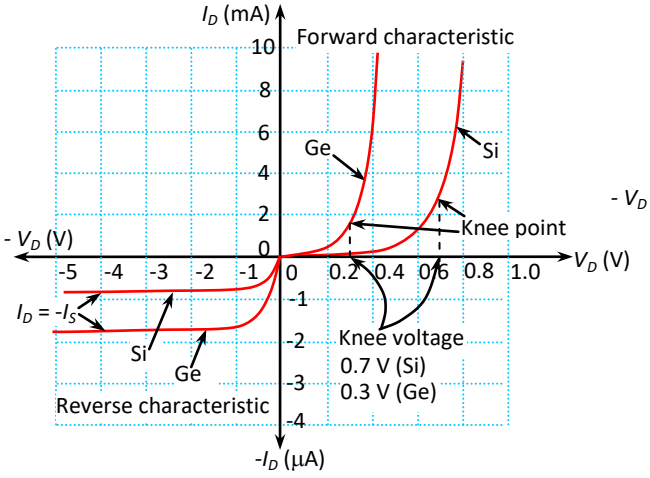


Fig.2-10: *I-V* Characteristic curve of a PN junction diode

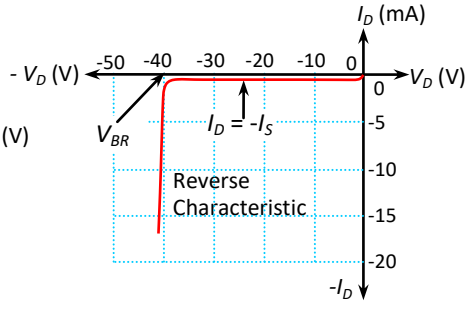


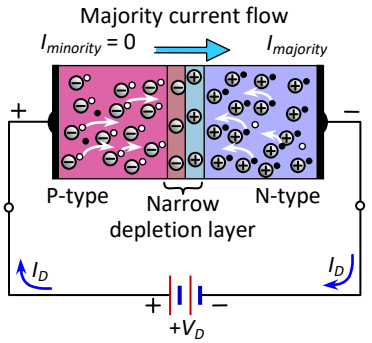
Fig.2-11: Breakdown voltage of reverse characteristic of a diode

The current that exists under reverse-bias condition is called the ***reverse saturation current*** (or ***dark saturation current***) and is represented by I_s (Fig.2-10). The value of I_s depends on the temperature. At 25 °C the value of I_S of a low power diode is typically 1 μA or less. For a very large value of reverse voltage, the reverse current increases suddenly and if the current is not controlled, the diode may be destroyed. The value of the reverse bias voltage for which the reverse current increases rapidly is called ***reverse breakdown voltage*** V_{BR} as shown in Fig.1-11.

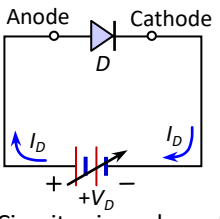
Characteristics in Forward Biased Condition

A forward bias is established by connecting the positive terminal of a battery to the P-type material and the negative terminal to the N-type material as shown in Fig.2-12. The application of a forward bias (V_D) will pressure electrons in the N-type material and holes in the P-type material to recombine with the ions near the boundary and reduce the width of the depletion

region as shown in Fig.2-12. The applied voltage will almost completely drop across the depletion layer. This forward voltage will produce an electric field which is in the opposite direction of original electric field of the barrier voltage.



(a) Circuit using constructional blocks of PN junction



(a) Circuit using schematic symbol of PN junction

Fig.2-12: Forward biased PN junction diode

Thus, the resultant electric field will decrease and the current due to minority carriers (minority drift current) will decrease and the majority current (diffuse current) will increase. If the applied forward bias voltage is equal to the barrier voltage (V_B), the resultant field in the depletion layer will be zero. Now, the minority carrier current will be zero and the majority carrier current will be high. In the forward bias condition, therefore, the forward current increases rapidly when the applied voltage is near about the barrier voltage V_B. The point of the *I-V* curve where the forward current increases rapidly is called ***knee point*** (Fig.2-10). After the knee point the current will increase rapidly with a very small increase in the forward voltage.

From the theory of solid-state physics, the general characteristics of a semiconductor diode can be defined by the following equation (Equ.2-1). This equation is referred to as Shockley's equation.

$$I_D = I_S \left(e^{\frac{qV_D}{nkT}} - 1 \right) \quad (2\text{-}1)$$

or,

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right) \quad (2\text{-}2)$$

where, I_s = reverse saturation current
q = magnitude of charge of an electron = 1.6×10^{-19} C
V_D = applied forward bias voltage to the diode
n = diode ideality factor, which is a function of the operating conditions and physical construction; its value has the range between 1 and 2 depending on a wide variety of factors (for simplicity, we will consider n = 1 unless otherwise stated).
k = Boltzmann's constant = 1.38×10^{-23} J/K
T = Absolute temperature

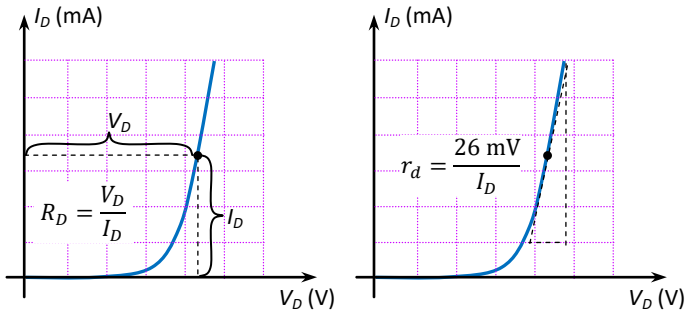


Fig.2-13: (a) DC resistance, and (b) AC resistance from *I-V* characteristics of PN junction

$V_T = \frac{kT}{q}$. V_T is called ***thermal voltage***. At 27° C or 300 K the value of V_T is 26 mV.

The DC resistance at any point of the input characteristics can be calculated using the following equation.

$$R_D = \frac{V_D}{I_D} \tag{2-3}$$

And, the AC resistance at any point can be calculated by using the following equation.

$$r_d = \frac{26\text{ mV}}{I_D} + r_B \tag{2-4}$$

Here, r_B is the bulk resistance of the PN junction which is very low and can be neglected.

2.8 Ideal Diode

In electronic circuits a PN junction diode is used as a switch that allows current only in one direction (forward direction). Although, a PN junction can behave as a one-way switch, in addition to switching property it has barrier voltage V_B, reverse saturation current I_S, junction capacitance (C_D) and some resistances (R_D). Actually these additional parameters are unwanted. An ideal diode is such a diode that provides only the one-way switching property, but will have no barrier voltage, reverse current, junction capacitance, and any resistance. Moreover, an ideal diode will have no limitation like – reverse breakdown, forward current limitation etc. The *I-V* characteristic curve of an ideal diode is given in Fig.2-14(a).

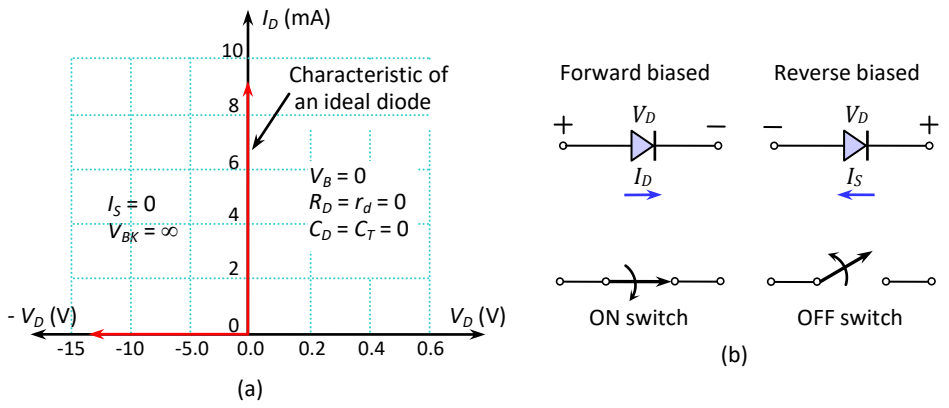


Fig.2-14: (a) Characteristics of an ideal diode, (b): Switch and ideal diode analogy

The operation of an ideal diode can be compared with that of a mechanical switch. If the diode is forward-biased, it works like a closed (ON) switch and if it is reverse-biased the diode works like an open (OFF) switch as shown in Fig.2-14(b). Though a mechanical switch can conducts current in both directions, a diode conducts current only in the forward direction.

2.9 Diode Equivalent Circuit

Neglecting the non-linearity of the characteristic curve, we can represent it by three straight lines [Fig.2-15(a)]. The equivalent circuit of the diode will be as shown in Fig.2-15(c). For this

characteristic, the equivalent circuit can be represented by a barrier voltage V_B, a resistance r_{av} and an ideal diode D connected in series as shown in Fig.2-15(c). Here, r_{av} is the average resistance of the portion of the characteristic curve after the knee point.

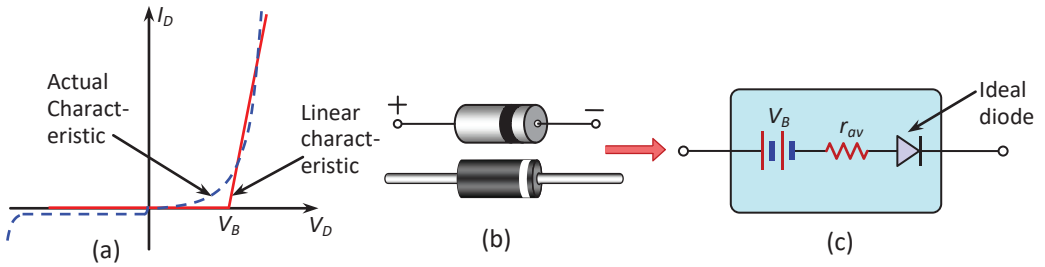


Fig.2-15: (a) Actual and linearized characteristics, (b) Actual diodes, and (c) Equivalent circuit of a diode

We know that the value of r_{av} is very small, typically less than 100 Ω. Hence in some operations, we can neglect this resistance. In that case, the equivalent circuit of the diode will consist of a barrier voltage V_B, and an ideal diode D connected in series as shown in Fig.2-16(b). The characteristic of this approximation will be as shown in Fig.2-16(a).

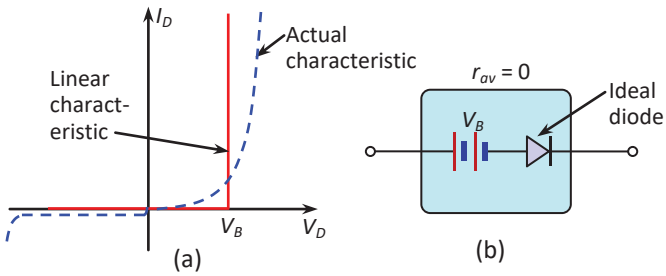


Fig.2-16: (a) Actual and linearized characteristics, and (b) Equivalent circuit of a diode an ideal diode

Even in some situations, where the external resistance is very high and the circuit operating voltage level is also very high compared to V_B, the operation of a practical diode can approximate to that of an ideal diode. Here, we neglect both r_{av} and V_B. The characteristic curve and the equivalent circuit are shown in Fig.2-17(a) and (b), respectively.

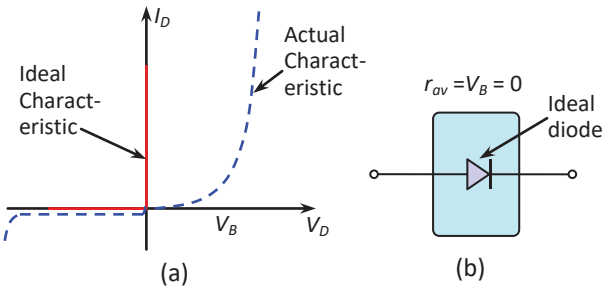


Fig.2-17: (a) Actual and linearized characteristics, and (b) Equivalent circuit of a diode

In these three equivalent circuits, the capacitance effect of the diode has not been considered. That is, these three equivalent circuits are considered DC equivalent circuits.

Equivalent Circuit with Capacitance

Every PN junction shows some capacitance effect (C_D). The capacitance of a PN junction is so small that in normal operation we can neglect it. But the capacitance becomes effective in very high frequency operation. Considering the junction capacitance, the equivalent circuit will be as shown in Fig.2-18.

2.10 Zener Diode

For a very large reverse bias voltage of a diode, the reverse current rapidly increases from reverse saturation current (breakdown). This phenomenon is used to produce a constant voltage device, called ***Zener diode***. There are two mechanisms that cause breakdown in reverse biased PN junction.

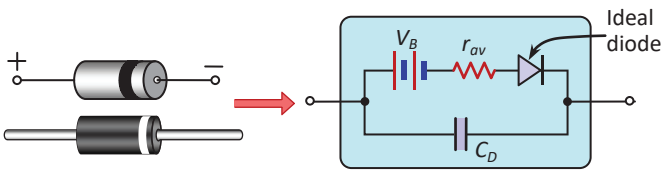


Fig. 2-18: AC equivalent circuit of a diode considering r_{av} and V_B

Zener Breakdown Mechanism

This type of breakdown takes place in the PN junction where the doping concentration is very high. Due to the high doping concentration, the width of the depletion layer will be comparatively small. So, for a particular reverse bias voltage, the electric field strength [V_D/(width of the depletion layer)] in the depletion layer, will be high enough to break away electrons from their atoms. With the breakdown of many such electrons insulating depletion layer converts into a conductor. This ionization by electric field is called ***Zener breakdown*** according to the name of its inventor. The Zener breakdown occurs usually with reverse bias voltage less than 5 V.

Avalanche Breakdown Mechanism

If the doping concentration of the PN junction is low the width of the depletion layer will be very large. So, when the reverse saturation current flows, the carriers travel a comparatively long distance and achieve large kinetic energies. If these energetic carriers collide with the electrons of covalent bonds of the crystal, the electrons become free. The newly developed free electrons also collide with other atoms and produce more free electrons. In this way, the carrier concentration in the depletion layer increases and the reverse current increases rapidly resulting in the junction breakdown. This breakdown mechanism is called ***avalanche breakdown***.

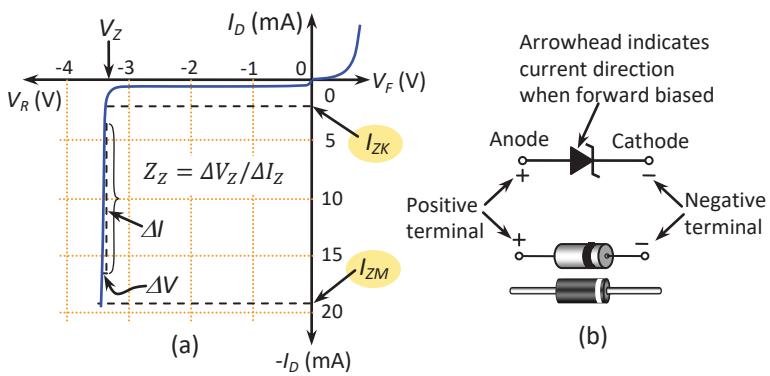


Fig.2-19: (a) Zener diode characteristics, (b) Symbol and practical diodes.

Characteristics of Zener Diode

Zener diode has almost the same characteristic as the normal low power rectifier diode except the lower value of reverse breakdown voltage. The typical characteristics of a Zener diode are shown in Fig.2-19(a) and the symbol of a Zener diode is shown in Fig.2-19(b).

In the reverse bias condition very small amount of reverse current flows. But after the Zener breakdown voltage V_Z, the reverse current increases rapidly. The operating point of a Zener diode may lie at any point of the reverse characteristic curve after breakdown. The Zener diode is used in circuit to produce a constant voltage (V_Z) and its performance depends on the shape of the reverse characteristics. The variation of this constant voltage with current depends on ***dynamic impedance*** of Zener diode (Z_Z) calculated as,

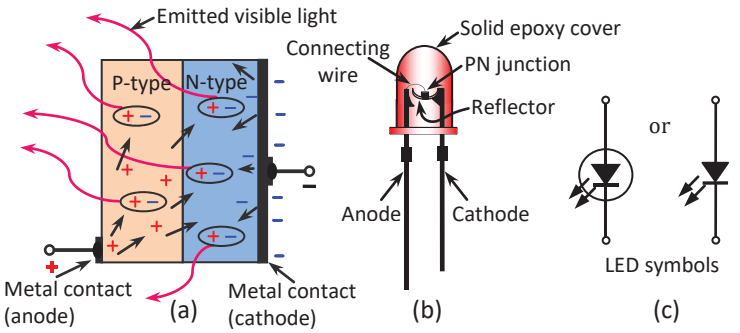


Fig.2-20: (a) Construction of LED using PN junction (b) Typical physical construction of LED (c) Symbols of LED

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} \qquad (2\text{-}5)$$

As illustrated in Fig.2-19(a) Z_Z defines how V_Z changes with the change of reverse current. The Zener diode current may be of any value between I_{ZK} and I_{ZM}. Here, I_{ZK} is the reverse current at the knee point of the reverse characteristic and I_{ZM} is the maximum Zener diode current which is limited by the power of a Zener diode.

2.11 Light Emitting Diode

Light emitting diode (LED) is a very common optoelectronic device used as an indicating device, nowadays as light source (LED tube lights, LED bulbs etc.). LEDs are also used to manufacture today's very high quality televisions, computer monitors and mobile phone displays. LED is nothing but a PN junction of suitable (direct band-gap) semiconductor materials. In a forward biased PN junction, light is emitted when the free electrons recombine with holes.

A cross-sectional view of an LED junction is shown in Fig.2-20(a). Instead of using a single semiconductor, alloys like gallium arsenide (GaAs), gallium phosphide (GaP), gallium arsenide phosphide (GaAsP) etc. are used for LED manufacturing. Combinations of different materials and ratio of different components produce different colors. To make an LED an N-type epitaxial layer is grown upon a substrate, and the P-region is created by diffusion method. The substrate is placed in a cup-type reflector that also works as the cathode connection as shown in Fig.2-20(b). The

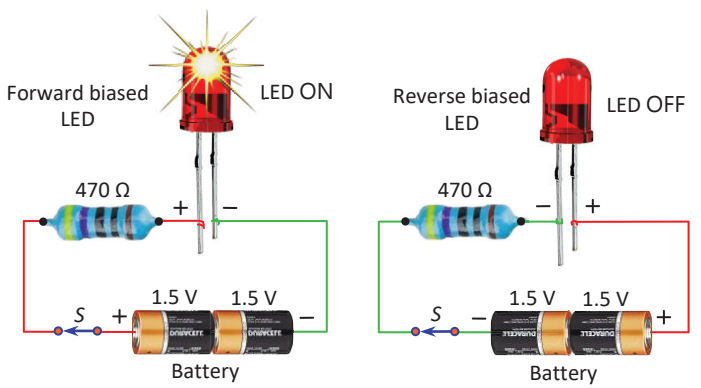
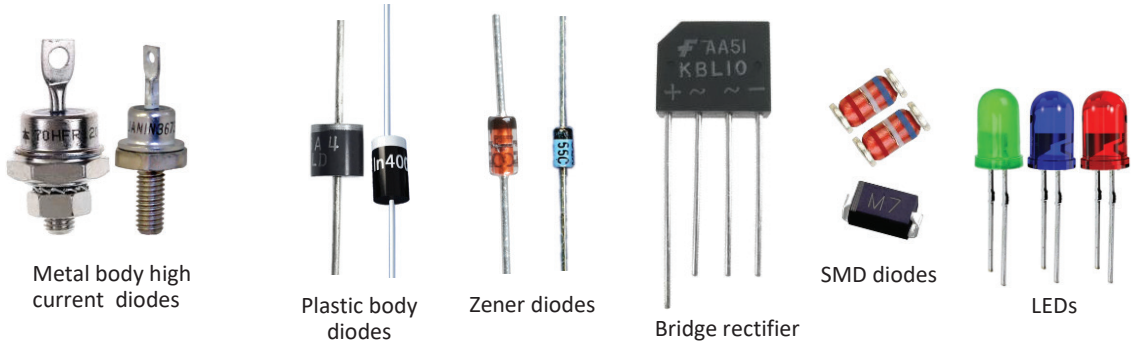


Fig.2-21: LED produces light when forward biased

positive (anode) lead is connected to P-type material by a very narrow wire. The whole arrangement is encapsulated in an epoxy lens (plastic cover).

Operation

When an LED is forward biased with a suitable voltage (about 1.5 V or more), a forward current flows through it. Electrons flow from N-side to the P-side and recombine with holes which are the majority carriers of P-type materials. When the free electrons come back to valence band from conduction band they emit their extra energy which is equal to band-gap energy (E_g). The extra energy is emitted as photons. By selecting suitable materials and changing their combination ration, band-gap energy (E_g) is changed and light of different color is produced.



Metal body high current diodes | Plastic body diodes | Zener diodes | Bridge rectifier | SMD diodes | LEDs

Fig.2-22: Photographs of different types of diodes

2.12 Applications of PN Junction Diodes

PN junction diodes are mainly used as rectifier, clipper circuits, clamper circuits etc. There are different types of rectifier circuits. Here, only two full wave rectifiers are described.

Full-Wave Rectifier

In ***half-wave rectifier***, the load gets power only for one half-cycle of the input AC power. That's why it has low DC and RMS value. But in a ***full-wave rectifier***, the load gets power for full-cycle of the input power. A full-wave rectifier with a centre-tapped transformer is shown in Fig.2.23. It uses two rectifier diodes and its input voltage is supplied from a transformer (T_1). The transformer must have a tape at the centre (CT).

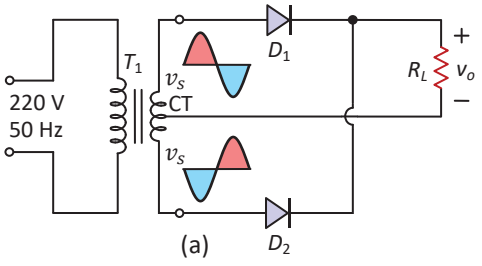


Fig.2-23: Two-diode full-wave rectifier

The function of the transformer is to step down 220 V AC power into required voltage, like 12 V, or 16 V etc. As shown in Fig.2-24(a), for the positive half cycle of input, the top-most terminal of centre-tapped transformer will be positive w.r.t. centre-tape, and the bottom-most terminal will be negative w.r.t. the centre-tape (at the secondary coil). For the negative half-cycle, the polarity will be just opposite [Fig.2-24(b)]. Both the secondary coils will produce same amount of AC voltage, $v_s = V_m \sin(\omega t)$.

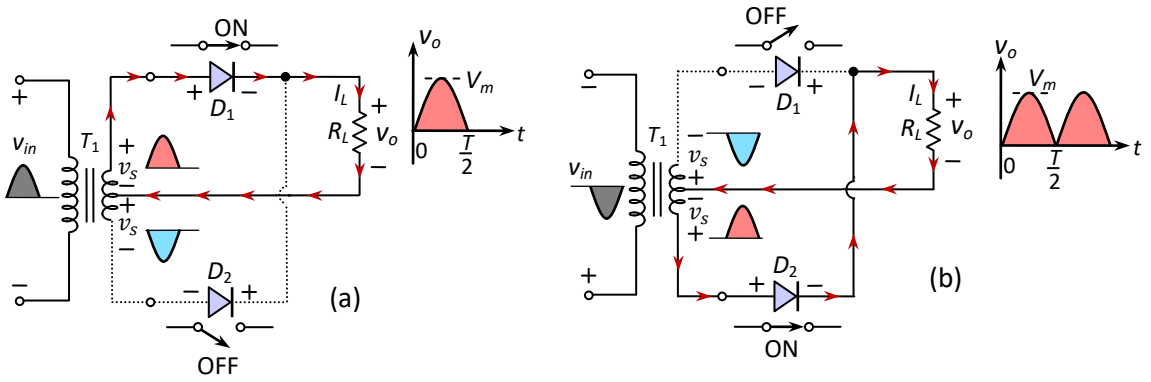


Fig.2-24: (a) Circuit status for the positive half-cycle (b) Circuit status for the negative half-cycle

During the positive half-cycle ($t = 0$ to $T/2$), the transformer output voltage is positive at the top. This positive terminal is connected to the anode of D_1, and the negative centre-tape is connected to the cathode of D_1 via R_L. Consequently, D_1 is forward biased, and load current, I_L, flows from top of the transformer secondary through D_1, through R_L (downward), and back to the transformer centre-tap. During this time, the polarity of the voltage from the bottom half of the transformer secondary causes diode D_2 to be reverse biased. Thus, D_1 behaves as short-circuit (ON) and D_2 behaves as open circuit (OFF) as shown in Fig.2-25(a). If the diode voltage drop is neglected the whole input voltage (transformer output voltage) will be developed across the load R_L.

During the negative half-cycle of the input ($t = T/2$ to T), the bottom-most terminal of the transformer secondary will be positive and the centre-tape will be negative. So, D_2 will be forward biased and behaves as short circuit as illustrated in Fig.2-25(a). Now, the load current flows from bottom of the transformer secondary through D_2, through R_L (from top to bottom), and back to the transformer centre-tape. As the polarity of the voltage of the upper half of the secondary has just reversed, diode D_1 will now be reverse biased and it will behave as open circuit.

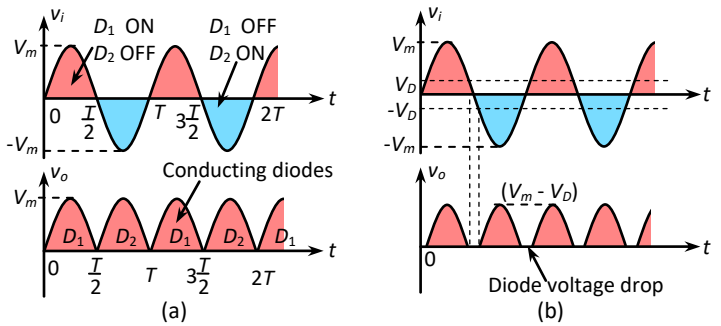


Fig.2-25: (a) Full-wave rectified output neglecting diode's barrier voltage V_D, and (b) Full-wave rectified output considering V_D

The direction of load current is always downward, that is, load is getting full-wave DC voltage. But the output is not pure DC, it is pulsating DC. If we neglect the voltage drop of the diodes the output waveform will be as shown in Fig.2-25(a). But, if we consider the voltage drop of the diodes the output wave form will be as shown in Fig.2-25(b). For both the positive and negative half-cycles, the voltage dropped across the reverse biased diode will be $2V_m$. So, the PIV (***peak inverse voltage***) rating of the diodes must be greater than $2V_m$.

The average DC output voltage of the full-wave rectifier will be,

$$V_{dc} = V_{avg} = \frac{2V_m}{\pi} \; or \; \frac{2(V_m - V_D)}{\pi} \qquad (2\text{-}4)$$

And the RMS output voltage will be,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \; or \; \frac{(V_m - V_D)}{\sqrt{2}} \qquad (2\text{-}5)$$

Full-Wave Bridge Rectifier

If the transformer does not have centre-tape then we have to use bridge rectifier circuit to get full-wave output.

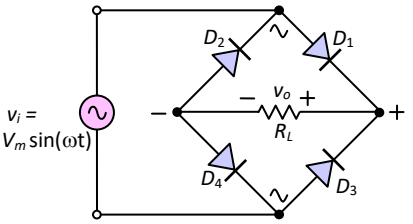


Fig.2-26: Full-wave bridge rectifier

The circuit diagram of a bridge rectifier is shown in Fig.2-26.

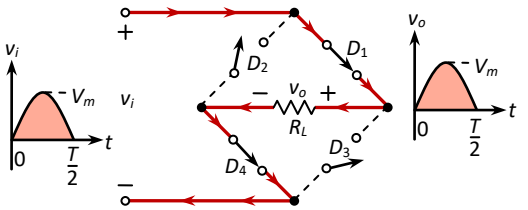


Fig.2-27: Circuit status for the positive half-cycle of input AC voltage

The bridge rectifier consists of four diodes connected with their arrowhead symbols all pointing toward the positive output terminal of the circuit. Among the four corners of a bridge rectifier two are AC input terminals and two are DC output terminal. The points at which anode of one diode and the cathode of one diode are connected are AC input terminals (marked by '~'). The terminal where the cathodes of two diodes are connected is the positive terminal of DC output (marked by '+'), and the point at which the anodes of two diodes are connected is the negative output terminal ('-').

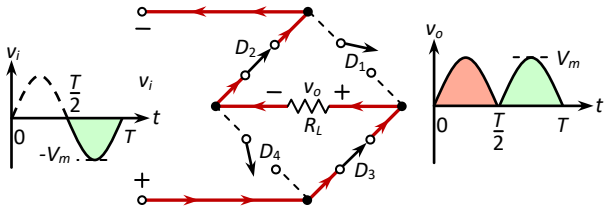


Fig.2-28: Circuit status for the negative half-cycle of input voltage

During the positive half-cycle of input voltage, diodes D_1 and D_4 become forward bias and conducts current (Fig.2-27). During the negative half-cycle of the input, diodes D_2 and D_3 are forward biased and conducts current (Fig.2-28). The output waveforms will be exactly same as the first rectifier and the same equations can be used. But the voltage drop will be double ($2V_D$ = 1.4 V) as the current passes through two diodes. Hence, $V_{dc} = V_{avg} = 2(V_m - 2V_D)/\pi$, and $V_{rms} = (V_m - 2V_D)/\sqrt{2}$.

2.13 Filters

In general a ***filter*** is a circuit that blocks a particular range of frequencies and passes other range of frequencies. In case of rectifier, the function of the filter circuit is to block the AC voltage and to pass the DC voltage to the load. There are different types of filter circuits. Here, the shunt capacitor filter is discussed.

As shown in Fig.2-29(a), a capacitor (C) connected at the output terminal across the load resistor (R_L) works as a good filter. For the positive half-cycle diode D_1 is forward biased and the capacitor is charged quickly to the peak value of input voltage, V_m. When the output voltage of the rectifier decreases from the peak value, the stored peak voltage of the capacitor reverse biases the diode, D_1. Now, the capacitor discharges through the load resistance R_L. Hence, the voltage decreases gradually. During the negative half-cycle, D_2 becomes forward biased and charges the capacitor to V_m voltage again. The process is continued and the output voltage across the load becomes smoother than the pulsating waveform. The output waveforms are shown in Fig.2-29(b).

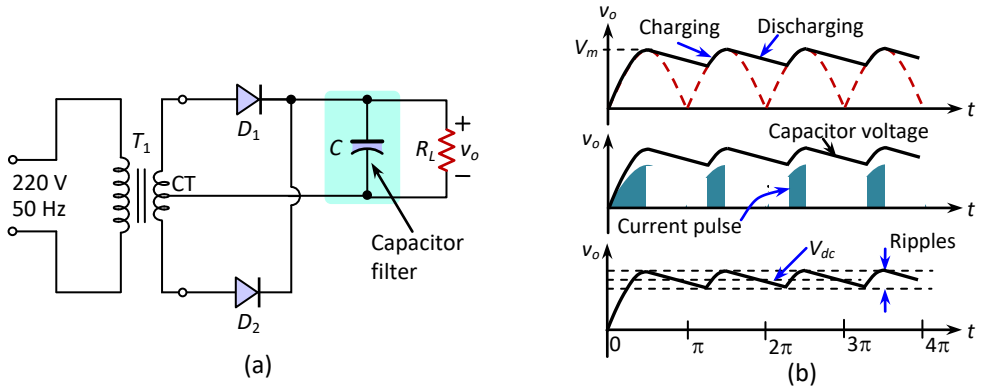


Fig.2-29: (a) Full-wave rectifier with capacitor filter, (b) Output waveform with capacitor filter

With the filter capacitor, the DC output voltage of this full-wave rectifier circuit will be,

$$V_{dc} = V_m \times \left(\frac{2fCR_L}{1 + 2fCR_L}\right) \tag{2-6}$$

2.14 Voltage Regulator Using Zener Diode

The output voltage of the power supplies described above (consisting of a transformer, a rectifier circuit, and a filter circuit) may vary due to the change of AC supply voltage and the load resistance. This variation can be reduced by using a ***regulator*** at the final stage (in between filter and the load). Although a lot of complicated circuits are employed as voltage regulator (discussed in Chapter 9), for a low power application Zener diode is commonly used. A simple regulator consists of a Zener diode and a series resistor as shown in Fig.2-30. The unregulated voltage (V_S) is applied to the input of the circuit and the regulated output voltage (V_o) is taken

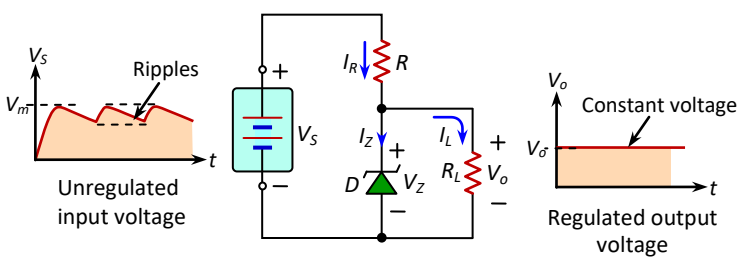


Fig.2-30: Application of Zener diode as voltage regulator

across the Zener diode. The regulated output voltage will be equal to the Zener breakdown voltage V_Z. The circuit will work properly if $V_S > V_o$. Resistor R limits the Zener diode current to the desired level and also drops the extra voltage $(V_R = V_S - V_o)$.

If the value of V_S increases the value of I_Z increases and the voltage drop across R (V_R) increases, but V_o remains constant. Similarly, if V_S decreases, I_Z decreases and the voltage drop V_R decreases and V_o remains constant again. On the other hand, if a load resistance is connected across the Zener diode, some current will be diverted from the Zener diode to the load. But the current through the resistor and hence voltage drop V_R will remain unchanged and so does the V_o. The value of I_Z has to be set to a suitable level [in between I_{ZK} and I_{ZM} as shown in Fig.2-19(a)].

2.15 Clipper Circuits

Clippers are one kind of electronic networks or circuits that clip off a portion of an input signal without distorting the remaining part of the signal. Clipper circuits are made using diodes and resistors and sometimes a voltage source. Depending on the orientation of the diode, the positive or negative portion of the applied signal is clipped off. So, there are two types of clippers: positive and negative clipper circuits. ***Positive clippers*** remove the positive portion of the applied signal and pass the negative portion. On the other hand, the ***negative clipper*** clips the negative portion of the applied waveform and keeps the remaining region as original one. Although, an unbiased clipper clips a complete half-cycle, by using suitable bias to the diodes, less than or more that one half-cycle can be clipped off.

Depending on the position of the diode, clippers are also called either series clipper or parallel clipper. In ***series clipper***, the diode is placed in series with the load resistance. But in ***parallel clipper***, the diode is connected in parallel with the load.

Fig.2-31 shows a ***biased series positive clipper*** and a ***biased series negative clipper*** circuit. Here, we will consider $0 < V < V_m$ and an ideal diode. Look at the polarity of the bias voltage (V). In the first circuit, it makes the diode forward biased, [Fig.2-31(a)]. Hence, even for no input voltage, that is, if the input terminals are short, the diode is still forward biased and $-V$ amount of voltage will be available at the output. That's why the output waveform starts from $-V$ volt. For the positive half-cycle of v_i, the forward bias voltage of the diode (that was effective for V voltage) will gradually decrease. It will be clear if we look at the polarity of the positive half-cycle and the polarity of bias voltage (they oppose each other). For this reason, the output negative voltage will gradually decrease. When the value of v_i is equal to bias voltage V, the resultant voltage across the diode will be zero, and hence the diode will not conduct any current through the load, and hence, the output voltage will be zero as shown in

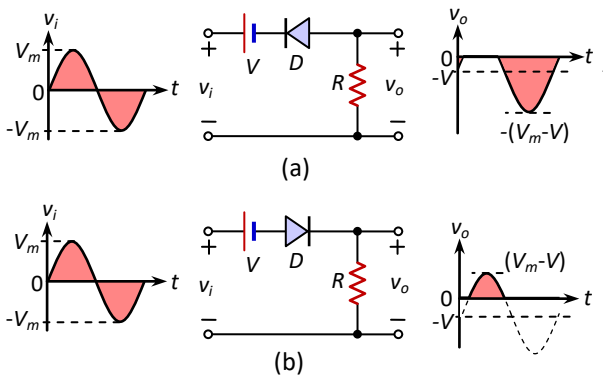


Fig.2-31: (a) Biased series positive clipper circuit, (b) Biased series negative clipper circuit

Fig.2-31(a). If the value of v_i exceeds V, the diode will be reverse biased by $(v_i - V)$ volts, and no output again. Thus, the output will be zero as long as $v_i > V$. During the falling edge of the positive half-cycle when $v_i = V$ the diode starts to conduct again, so we will get negative output voltage. During the negative half-cycle of the input, v_i will be added with V and forward bias the diode. Thus negative output will be available across the load from $v_i = V$ up to $v_i = -V_m$. For this reason the negative peak will be $-V_m - V = -(V_m + V)$, which is shown in output waveform of Fig.2-31(a).

In the 2nd circuit, the direction of the diode is just opposite. So the bias voltage (V) will reverse biases the diode. The diode will block the negative voltage and pass the positive voltage. But due to the reverse bias voltage, V, the full positive half-cycle will not be found at the output. The maximum output voltage will be only $V_m - V$ as shown in Fig.2-31(b).

2.16 Clamper Circuits

A ***clamper*** circuit, constructed of a diode, a resistor, and a capacitor, shifts a waveform to a different DC level without changing the shape of the signal. That is, a clamper circuit adds a DC level in the output signal. Depending on the direction of shifting, clamper circuits are classified as: ***positive clampers*** and ***negative clampers***. Both of them may be either biased or unbiased. Thus, there are four types of clampers:

1. Simple negative clamper
2. Simple positive clamper
3. Biased negative clamper
4. Biased positive clamper

Simple Negative Clamper

The circuit diagram of a simple negative clamper is shown in Fig.2-32(a). To easily understand the operation of any clamper circuits, first we have to consider the half-cycle that forward biases the diode. Here, for the positive half-cycle of the input signal $(0 \rightarrow \frac{T}{2})$, the diode will be forward biased and the capacitor will be charged by V_m with +ve on the left side as shown in Fig.2-32(b). As the diode is short (neglecting barrier voltage), the voltage across the load resistance will be zero. However, during the negative half-cycle $\left(\frac{T}{2} \rightarrow T\right)$, the diode is reverse biased. So it will behave as

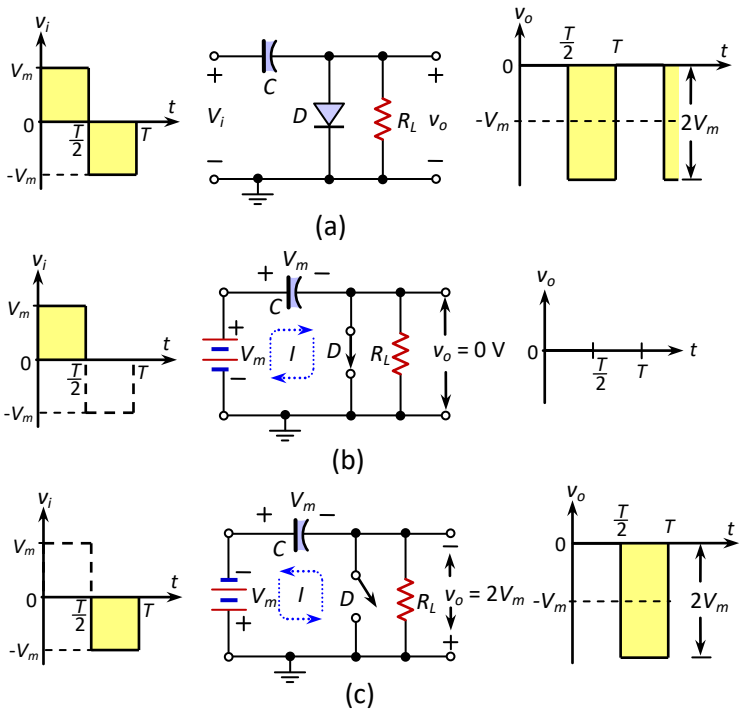


Fig.2-32: (a) Negative clamper circuit (unbiased), (b) Operation for positive half-cycle, and (c) Operation for negative half-cycle

an open circuit as shown in Fig2-32(c). For this situation, the value of output voltage can be obtained using KVL as,

$$-V_m - V_m + v_o = 0 \quad \therefore v_o = 2V_m$$

That is, the output voltage will be the sum of the capacitor voltage and source voltage with positive at the bottom. Thus, we will get $v_o = -2V_m$. Observe that, the input signal has been shifted to negative direction by a value of V_m. Or we can say a DC value of $-V_m$ has been added to the output waveform.

2.17 Testing Diode Using Multimeter

Sometimes it is necessary to test a diode to confirm whether it is OK or not. Using multimeter, we can do that. There are two ways to test a diode. We can use 'Diode Test' mode (shown by a diode symbol on the meter) of the multimeter, or if the multimeter has no 'Diode Test' option, we can use 'Resistance Test' option (shown by the ohm symbol). Here only the first method is discussed.

If we want to test a diode that is already connected in a circuit, we have to disconnect it, or disconnect at least one terminal of the diode from the circuit. For safety, the power supply of the circuit must be switched OFF. Moreover, we have to be careful about the high voltage stored in the capacitors or inductors!

As shown in Fig.2-33, the selector knob of the multimeter has to be set on 'Diode Test' position (indicated by a diode symbol). A good forward-based diode displays a voltage ranging from 500 mV to 800 mV for Si diode. But for germanium diodes the voltage range should be 200 mV to 300 mV. On the other hand, a reverse biased diode will show 'OL' reading. If the diode is not OK, it may be ***short*** or ***open***. An open diode will also give 'OL' reading for both forward bias and reverse bias conditions. On the other hand, a short diode may give 0 V or very small voltage (300 mV for Si) in both directions.

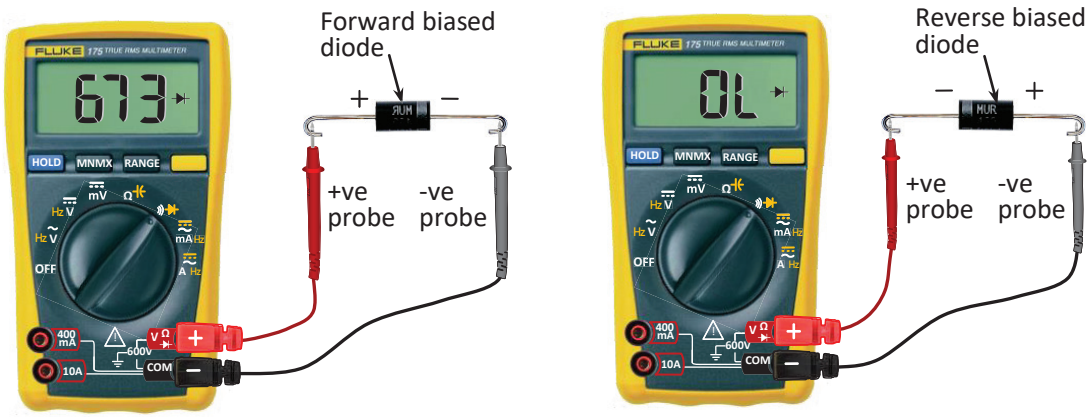


Fig.2-33: (a) Forward bias testing, and (b) Reverse bias testing using multimeter

CHAPTER
3

Bipolar Junction Transistor (BJT)

3.1 Introduction

In electronics, transistor is the most widely used device. The transistor was invented on December 23, 1947 at Bell Laboratories by William Shockley, John Bardeen and Walter Brattain[1]. Since then the applications of transistors are gradually increasing either in discrete form or in IC (Integrated Circuit) form. This chapter will discuss the construction and operations of transistors.

3.2 Construction of a Transistor

A bipolar junction transistor (simply called transistor) consists of two back-to-back PN junctions manufactured in a single piece of semiconductor material. It is constructed by sandwiching a P layer in between two N-layers as shown in Fig.3-1. This type of transistor is called an ***NPN transistor***. Alternately, a transistor can be manufactured by sandwiching an N-layer in between two P-layers as in Fig.3-2. This configuration is called a ***PNP transistor***.

The middle layer is called the ***base*** (*B*), of the remaining two layers one is called the ***emitter*** (*E*) and the other is called the ***collector*** (*C*). Terminal leads are attached to each layer of the transistor. The emitter and collecter layers are heavily doped (concentration of impurity atoms is high), but the base layer is lightly doped (concentration of impurity atoms is low). The outer layers have widths much greater than the sandwiched P or N-type layer. The actual dimension of transistor may vary from 10 to several 10s of microns. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 1:10 or less).

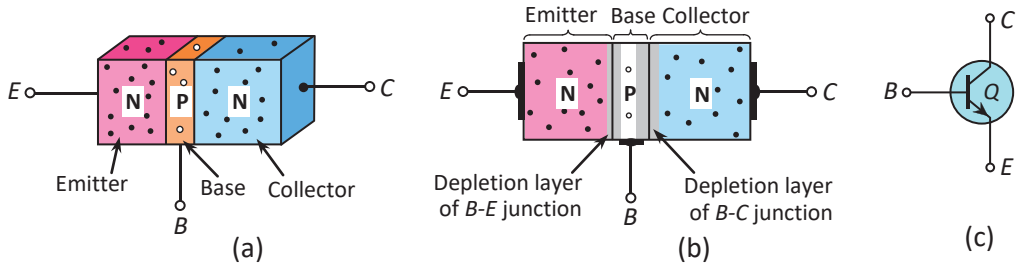


Fig.3-1: Construction of NPN transistors, (a) Three-dimensional block, (b) Two-dimensional block, and (c) Symbol of an NPN transistor

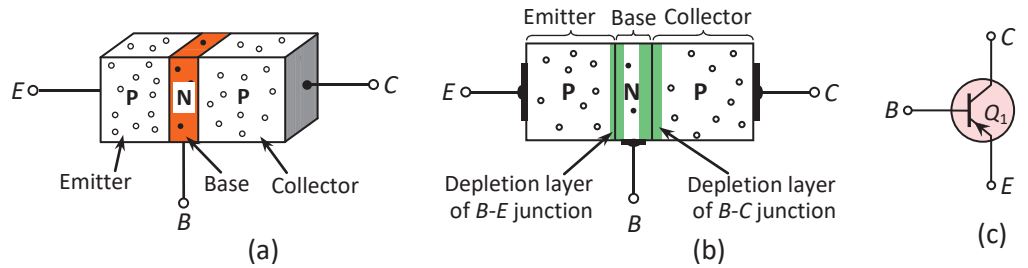


Fig.3-2: Construction of PNP transistor, (a) Three-dimensional block, (b) Two-dimensional block, and (c) Symbol of a PNP transistor

Fig.3-1 and Fig.3-2 show the block diagrams and symbols of NPN, and PNP transistors, respectively. Look at the symbols of the transistors. The base terminal is in the middle and the collector and the emitter are connected to the base. Emitter is differentiated from the collector by an arrow. In NPN transistor the arrow direction is outward from the base and in PNP transistor the direction of the arrow is towards to base. This arrow direction indicates the direction of conventional current in the emitter terminal.

3.3 Operation of a Transistor

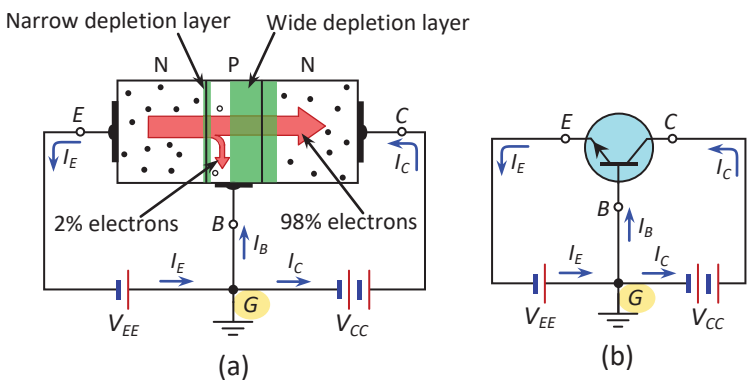


Fig.3-3: Operation of an NPN transistor, (a) Circuit with transistor block, and (b) Circuit with transistor symbol

Here, the operation of an NPN transistor is described [Fig.3-3(a)]. For proper functioning of a transistor, the base-emitter junction (*B-E* junction) must be forward biased and the base-collector junction (*B-C* junction) must be reverse biased as shown in Fig.3-3. So, the negative voltage to the emitter and the positive voltage to the collector have been supplied with respect to the base. The base is common to

both the input circuit (*B-E* circuit) and the output circuit (*B-C* circuit), hence this configuration is called ***common base configuration*** (CBC).

Due to the forward bias, the depletion layer of *B-E* junction is reduced, that results in a heavy flow of majority carriers electrons from N-type emitter to P-type base material. These injected electrons are the minority carriers in P-type base. Due to the reverse bias, the depletion layer of the *B-C* junction is widened. The electric field of reverse biased *B-C* junction attracts the electrons injected by the emitter (which are the minority carriers in base region) and most of them manage to reach the collector layer. As the base is lightly doped and its width is very small, only a few of the electrons recombine with the majority holes in the base. For example, if 100 electrons are injected by the emitter per second, less than 2 electrons will recombine in the base and more than 98 will move to the collector. The direction of conventional current is just opposite to the direction of electrons flow. So, a current will be produced from emitter to battery which is called emitter current I_E. Due to the recombination of 2 holes (with 2 electrons) a small base current (I_B) will flow into the base. On the other hand, 98 electrons that move to the collector, constitute the injected collector current $I_{C(INJ)}$ and its direction is from the battery to the collector as shown in Fig.3-3. Now, if we apply KCL at point G, we have

$$\boxed{I_E = I_{C(INJ)} + I_B} \qquad (3\text{-}1)$$

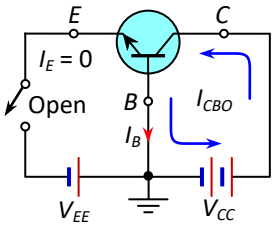


Fig.3-4: Collector leakage current with emitter open

From this operation it is now clear that more that 98% of the emitter current is transferred to the collector and only less than 2% is lost in the base. This current transfer action is called the ***transistor action***. Due to the forward bias, *B-E* circuit has very low resistance and due to the reverse bias the *B-C* circuit has very high resistance. But the transistor has transferred the current from the low resistance circuit to the high resistance circuit. That is why, this device is called "***trans***fer-re***sistor***" or "***transistor***". The ratio of the injected collector current to the emitter current is called the ***current gain*** (***α***) of a transistor in common base configuration (CBC). That is,

$$\boxed{\alpha = \frac{I_{C(INJ)}}{I_E}} \qquad (3\text{-}2)$$

or ,
$$\boxed{I_{C(INJ)} = \alpha I_E} \qquad (3\text{-}3)$$

The value of α is less than unity and ranges from 0.95 to 0.997.

The $I_{C(INJ)}$ is not only the current component in the collector. In the reverse bias *B-C* junction a leakage current flows due to the thermally generated minority carriers even if the emitter terminal is open (shown in Fig.3-4.). This current is denoted as I_{CBO}, ***C***ollector to ***B***ase current with emitter ***O***pen. Thus, the collector current I_C will have two components as,

$$I_C = I_{C(INJ)} + I_{CBO} \qquad (3\text{-}4)$$

or,
$$I_{C(INJ)} = I_C - I_{CBO}$$

$\therefore$
$$\boxed{\alpha = \frac{I_{C(INJ)}}{I_E} = \frac{I_C - I_{CBO}}{I_E}} \qquad (3\text{-}5)$$

But as the value of I_{CBO} is very small it can be neglected, that is $I_C = I_{C(INJ)}$.

Therefore we can write

$$\alpha = \frac{I_{C(INJ)}}{I_E} \approx \frac{I_C}{I_E} \qquad (3\text{-}6)$$

Using Equ.(3-4) and (3-6) , we can also write,

$$\boxed{I_C = \alpha I_E + I_{CBO}} \qquad (3\text{-}7)$$

Again, if we apply KCL at point G, we get,

$$\boxed{I_E = I_C + I_B} \qquad (3\text{-}8)$$

Operation of a PNP transistor is exactly same, except here holes move from emitter to collector through base, instead of electrons. The biasing voltages of the PNP transistor will also be in reverse direction as shown in Fig.3-5.

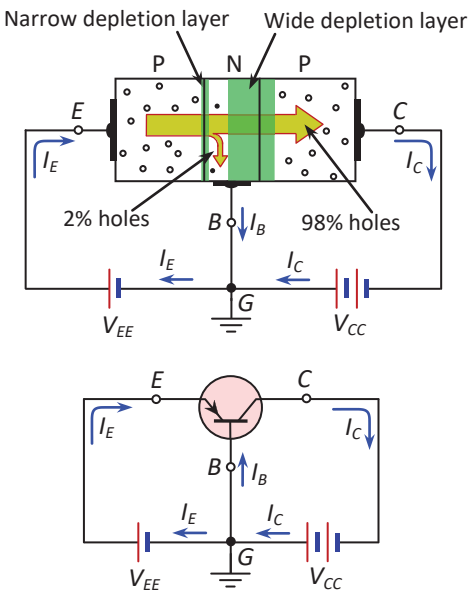


Fig.3-5: Operation of a PNP transistor

3.4 Amplifying Action of a Transistor

The capacity of a transistor to transfer a signal from a low resistance circuit to a high resistance circuit is the key factor for voltage amplification. As shown in Fig.3-6, even if we connect a large resistor, *R*, (say 2 kΩ) at the collector circuit, transistor action will not be hampered, i.e., more than 98% of the emitter current will be transferred to the collector. Now let us consider that the emitter bias voltage $V_{EE} = 1$ V and the forward resistance of the *B-E* junction is $r_{in} = 50\ \Omega$. So in the emitter circuit I_E will be,

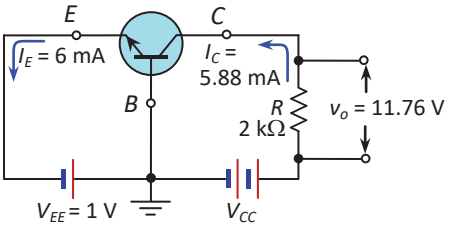


Fig.3-6: Amplifying action of transistor

$$(V_{EE} - V_{BE}) \div r_{in} = (1\text{ V} - 0.7\text{ V}) \div 50\ \Omega = 6\text{ mA}$$

Due to the transistor action 98% of this current will be transferred to the collector. So, I_C will be 5.88 mA. If we take the output voltage (V_o) across the external resistor *R*, according to Ohm's law its value will be $5.88\text{ mA} \times 2\text{ k}\Omega = 11.76$ V! By applying 1 V in the input circuit we have found 11.76 V at the output. In this way, a transistor increases the input voltage level at the output. Here, DC voltage has been amplified. Transistor is mostly used for AC voltage amplification.

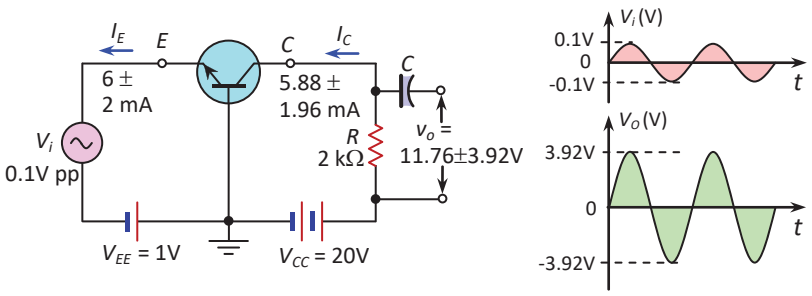


Fig.3-7: AC amplification using transistor

As shown in Fig.3-7, if we connect an AC source of very small voltage, say $V_i = 0.1 \sin \omega t$, in series with the biasing voltage V_{EE}, an AC current will also flow in the emitter circuit. In this case the peak value of the AC current will be $(0.1\text{V} \div 50\ \Omega) = 2\ \text{mA}$. So, the peak value of the AC current in the collector circuit will be $1.96\ \text{mA}$ ($2\text{mA} \times 98\%$). The AC peak voltage across the resistor will be $3.92\ \text{V}$ ($1.96\ \text{mA} \times 2\text{k}\Omega$) as shown in the figure. The output will have a DC voltage level which will not pass through the capacitor. In this way, a transistor can amplify AC voltage also.

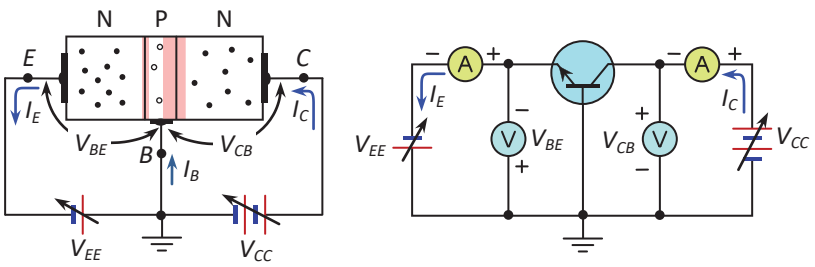


Fig.3-8: Circuit for determining transistor characteristics in CBC

Although, a transistor in CB configuration (as in Fig.3-6 and 3-7) provides voltage amplification, it cannot produce current amplification as the output current I_C is less than the input current I_E. However, there are some other configurations (CEC, CCC) that can produce current amplification.

3.5 Characteristics of a Transistor

For any device, *I-V* characteristics are very important to understand the operation of that device. As a transistor has three terminals, keeping any one terminal common to the input and output circuits three configurations are possible. These are

a) **C**ommon **B**ase **C**onfiguration (**CBC**)
b) **C**ommon **E**mitter **C**onfiguration (**CEC**) and
c) **C**ommon **C**ollector **C**onfiguration (**CCC**)

3.6 Characteristics of a Transistor in CBC

In common base configuration (CBC), the base is common to the input and output circuits. The emitter-base constitutes the input circuit, and the base-collector constitutes the output circuit. The base-emitter voltage (V_{BE}) is the input voltage and the emitter current (I_E) is the input current. Similarly, the base-collector voltage (V_{CB}) is the output voltage and the collector current (I_C) is the output current. We have to study the characteristics of both input and output circuits. Here, we will discuss them for an NPN transistor. The characteristics of PNP transistor will exactly be same but the polarity of bias voltage and the current directions will be just opposite.

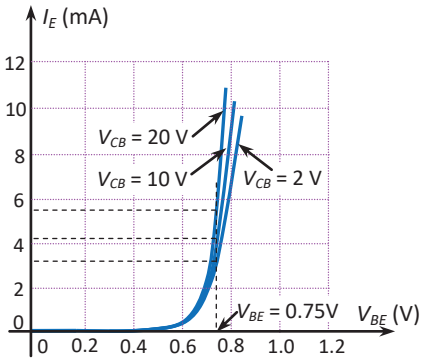


Fig.3-9: Common-base input characteristic (NPN)

Input Characteristics

To draw the input characteristic curve, the value of V_{BE} is gradually changed and the value of I_E is measured keeping V_{CB} constant, using the circuit of Fig.3-8. By plotting the data on a $V_{BE} - I_E$ coordinate system an input characteristic curve is found. The process is repeated for different values of V_{CB}.

A family of input characteristic curves for an NPN transistor is shown in Fig.3-9. Since the input is across the forward biased base-emitter junction, the input characteristics have exactly the same shape as that of a forward biased PN junction. For a silicon transistor the value of I_E is almost zero up to $V_{BE} = 0.5$ V. After that voltage, I_E stats to increase and has a knee point at $V_{BE} = 0.7$ V. For a germanium transistor the value of knee voltage will be 0.3 V.

The shape of these $I_E - V_{BE}$ curves also depends on the output voltage V_{CB}. As shown in the figures, I_E increases with the increase of V_{CB}.

Example 3-1:

Calculate the DC resistance and AC resistance for $V_{BE} = 0.75$ V on the input characteristics of a transistor in CB configuration shown in Fig.3-10. Assume, $r_B = 2\ \Omega$.

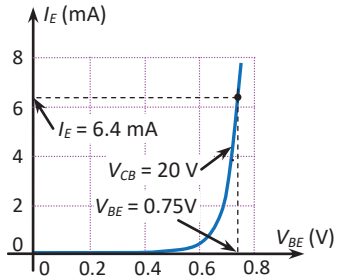


Fig.3-10: Input graphs for Example 3-1.

Solution:

First, we have to draw a vertical line on $V_{BE} = 0.75$ V (as shown on the figure). Then we have to find the intersecting point of this vertical line with the graph. Now, if we draw a horizontal line through this point it will intersect the y-axis. This intersecting point gives the value of I_E, which is ≈ 6.4 mA.

Now, using Equ.(2-3), the value of DC resistance can be calculated as,

$$R_D = \frac{V_D}{I_D} = \frac{V_{BE}}{I_E} = \frac{0.75\text{ V}}{6.4\text{ mA}} \approx 117\ \Omega\ (\text{Ans.})$$

Using Eq.(2-4), the value of AC resistance is,

$$r_d = \frac{26\text{ mV}}{I_D} + r_B = \frac{26\text{ mV}}{I_E} + r_B = \frac{26\text{ mV}}{6.4\text{ mA}} + 2\ \Omega \approx 6\ \Omega\ (\text{Ans.})$$

Comments: The formulas for PN junction diode have been used here, as the *B-E* junction of a transistor has a forward biased PN junction.

Output Characteristics

The output characteristics can be determined using the same schematic diagram of Fig.3-8. For this purpose, the collector (output) current, I_C, is measured as the output voltage V_{CB} is adjusted with a fixed value of input (emitter) current I_E. When the measured data are plotted on an I_C versus V_{CB} coordinate system, we get output characteristic curve. By repeating the process for different fixed values of I_E we can draw a family of output characteristic curves as shown in Fig.3-11.

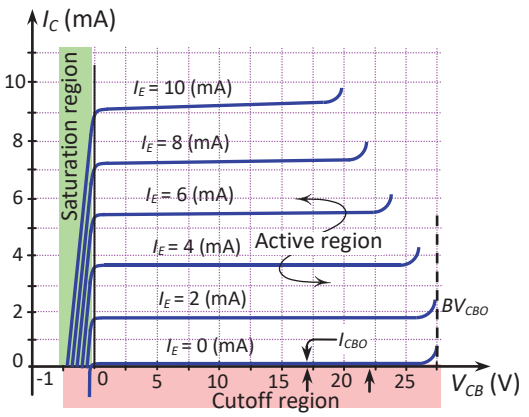


Fig.3-11: Common-base output characteristics (NPN)

From Fig.3-11, it is clear that each curve stats from the left side of $V_{CB} = 0$ line (y-axis) and increases rapidly just as V_{CB} increases slightly from its negative value. At $V_{CB} = 0$, I_C becomes almost equal to I_E and the ratio I_C / I_E is called the current gain, α, in *CBC*. Afterwards, the curves become almost parallel to x –axis which means that I_C becomes constant.

This family of output characteristic curves has three regions. These are: ***saturation region***, ***cutoff region***, and ***active region***.

The region where the value of I_C increases with the increase in V_{CB}, is called the ***saturation region***. Certainly, this region is to the left of $V_{CB} = 0$ line (or y-axis). In this region both the *B-E* and the *B-C* junctions are forward biased.

As we know, when the emitter terminal is open, i.e., when $I_E = 0$, a very small current I_{CBO} flows through the collector. On the output characteristic curve this line passes almost along the x-axis. The region below this curve is called the ***cutoff region***. In this cutoff region both the junctions are reverse biased. The cutoff and saturation regions are used when a transistor works as a switch.

The region in between the saturation and the cutoff regions is called the ***active region***. In this region, the *B-E* junction is forward biased (as $I_E > 0$) and the *B-C* junction is reverse biased by V_{CB}. This is the region where a transistor works as an amplifier. In this region, with a very large change in the output voltage, V_{CB}, practically no change is found in I_C. This ensures a very large output resistance of the transistor in active region ($r_O \approx \infty$).

In addition to these three regions, there is another region called ***breakdown region***, were we should not operate a transistor because in this region the transistor breaks down (burns out).

3.7 Characteristics of a Transistor in CEC

In ***common emitter configuration*** (CEC), the emitter is common to both input circuit and output circuit as shown in Fig.3-12. The base-emitter voltage V_{BE} is the input voltage and the base current I_B is the input current. On the other hand, collector-emitter voltage, V_{CE}, is the output voltage and the collector current I_C is the output current. For proper understanding of this configuration we have to describe some parameters and expressions.

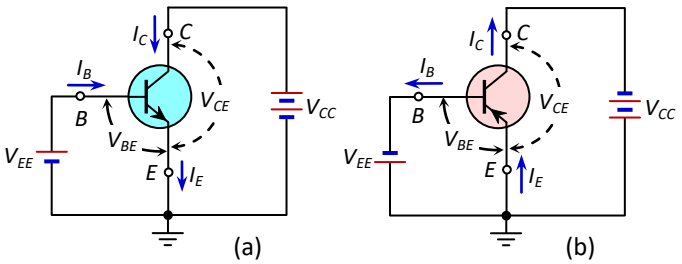


Fig.3-12: Common emitter configuration circuits
(a) NPN (b) PNP

Current Gain Beta (β)

Unlike the CB configuration CE configuration gives high current gain which is defined as the ratio of the output current, I_C, to the input current, I_B, and is denoted by ***beta*** (β). It can be measured for both DC current and AC current as,

$$\beta_{dc} = \frac{\text{DC output current}}{\text{DC input current}} = \frac{I_C}{I_B} \tag{3-9}$$

The value of β_{dc} is much greater than unity and depends on the value of α_{dc}.

$$\boxed{\beta_{ac} = \frac{\text{Change in } I_C}{\text{Change in } I_B}\Big|_{V_{CE}(\text{constant})} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}(\text{constant})}} \quad (3\text{-}10)$$

β_{ac} is also called ***common-emitter forward-current amplification factor***. On datasheets β_{dc} is normally referred to as h_{FE} and β_{ac} is referred as h_{fe}.

Relation Between α and β

From transistor action, we find

$$I_E = I_{C(INJ)} + I_{CBO} + I_B = I_C + I_B \; [\because I_{C(INJ)} + I_{CBO} = I_C]$$

Dividing both side of this equation by I_C, we get

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$or, \quad \frac{1}{I_C/I_E} = 1 + \frac{1}{I_C/I_B}$$

$$[\because \frac{I_C}{I_E} \approx \alpha \text{ and } \frac{I_C}{I_B} = \beta]$$

$$\therefore \quad \frac{1}{\alpha} = 1 + \frac{1}{\beta} \quad or, \quad \frac{1}{\alpha} - 1 = \frac{1}{\beta}$$

$$or, \quad \frac{1-\alpha}{\alpha} = \frac{1}{\beta}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \quad (3\text{-}11)$$

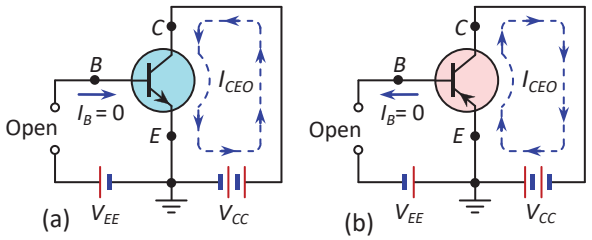


Fig.3-13: Leakage current in CEC (a) NPN, and (b) PNP transistor.

Leakage Current in CEC (I_{CEO})

Like the CB configuration, CE configuration also produces a leakage current due to the thermally generated minority carriers. Fig.3-13 shows CE circuits where the base-emitter circuits are open but the reverse biasing voltage sources (V_{CC}) remain connected. The only current that can flow is the minority carriers reverse current through the *C-B* junction. It is designated as I_{CEO}; ***C***ollector to ***E***mitter current with the base ***O***pen. Although, it is called 'reverse' current it flows in the same direction as the majority carriers collector current. I_{CEO} is directly related to I_{CBO}. The relation is,

$$\boxed{I_{CEO} = (\beta + 1) I_{CBO}} \quad (3\text{-}12)$$

And the expression of the collector current will be,

$$\boxed{I_C = \beta I_B + I_{CEO}} \quad (3\text{-}13)$$

Example 4:

Applying appropriate biasing voltage in a PNP germanium transistor, two ammeters are connected to the collector and base. The readings of the meters are 61 mA and 0.4 mA, respectively. If the value of β of the transistor is 150, calculate the leakage currents, I_{CEO} and I_{CBO}.

Solution:

Since the reading of the two ammeters are 61 mA and 0.4 mA, the value of $I_C = 61$ mA and $I_B = 0.4$ mA.

We know that [Equ.(3-13)],

$$I_C = \beta I_B + I_{CEO}$$

$$or, \quad I_{CEO} = I_C - \beta I_B$$

$$or, \quad I_{CEO} = 61 \text{ mA} - 150 \times 0.4 \text{ mA} = 1 \text{ mA [Ans.]}$$

Again we know that [Equ.(3-12)],

$$I_{CEO} = (\beta + 1) I_{CBO}$$

$$or, \quad I_{CBO} = \frac{I_{CEO}}{\beta + 1} = \frac{1 \text{ mA}}{150 + 1} \approx 6.62 \text{ μA [Ans.]}$$

Comments: The value of leackage current (I_{CEO}) is larger in CEC than that in CBC (I_{CBO}).

Input Characteristics

The input characteristic shows the relation between the input current, I_B, and the input voltage, V_{BE}, for a fixed value of collector-emitter voltage, V_{CE}. The arrangement is shown in Fig.3-14. V_{BE} is gradually changed and I_B is measured for a constant value of V_{CE} using the variable source V_{BB}. By plotting the data on a $V_{BE} - I_B$ coordinate system an input characteristic curve is found. The process is repeated for different values of V_{CE}. The ***family of input characteristic curves*** are shown in Fig.3-15.

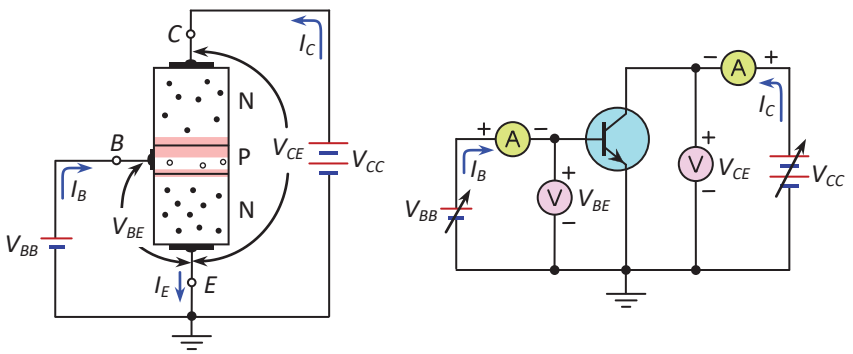


Fig.3-14: Circuit for determining transistor characteristics in CEC

The shape of the input characteristic curves resembles that of the CB configuration. The only difference is, input current I_B decreases with the increase of output voltage V_{CE}.

Output Characteristics

The output characteristics can be determined using the same circuit of Fig.3-14. For determining this characteristics, the output voltage, V_{CE}, is gradually changed and the output current, I_C, is measured for different fixed values of input current, I_B. When the measured data are plotted on an I_C versus V_{CE} coordinate system, we get a family of output characteristic curves (Fig.3-16).

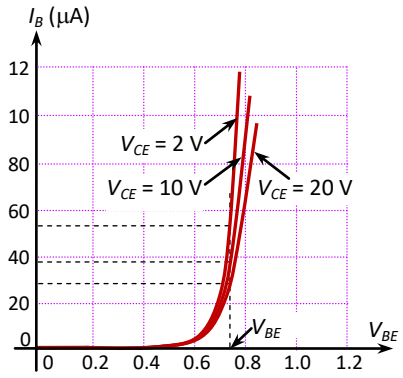


Fig.3-15: Common-emitter input characteristic (NPN)

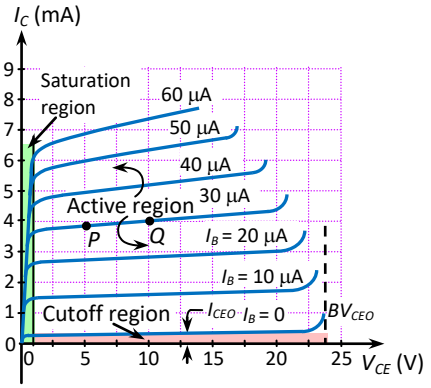


Fig.3-16: Common-emitter output characteristics (NPN)

Here, also the graph has three regions. The region where I_C increases with V_{CE} is called the ***saturation region***. In the saturation region, both the junctions of the transistor are forward biased. The region below the $I_B = 0$ line is called the ***cutoff region*** where, both the junctions are reverse biased. The area in between the saturation region and cutoff region, where the curves are more or less parallel to the x-axis is called the ***active region***.

3.8 Transistor Biasing Circuits

DC Load Line and Operating Point

As discussed before, a transistor can work at different points (regions) of its characteristic curve. ***Operating point*** is the values of output current and voltage actually a transistor works on. For a fixed value of bias voltage and output resistance (or load resistance) operating point can be at any location within a line on the output characteristics. This line is called the ***load line***. Or, the line, drawn on the transistor output characteristics, that gives all possible positions of the operating point is called the ***load line***.

To draw a load line we will consider a common-emitter (CE) circuit as shown in Fig.3-17. We need an expression that relates I_C and V_{CE}. This can easily be found from the *C-E* circuit of Fig.3-17. By applying KVL to *C-E* loop of this circuit we get,

$$V_{CC} - I_C R_L - V_{CE} = 0 \qquad (3\text{-}14)$$

or,

$$\boxed{V_{CE} = V_{CC} - I_C R_L} \qquad (3\text{-}15)$$

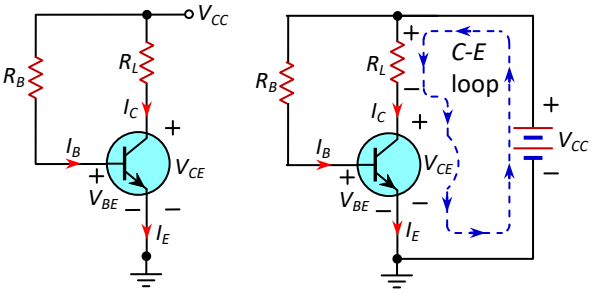


Fig.3-17: Transistor Circuit for determining load line.

Equ.(3-15) is an equation of straight line, and the line represented by this equation is called the load line, as defined before. To draw this line on the output characteristics of the transistor we have to determine two points. Let's do that.

Point A (V_{cc}, 0):

When, $I_C = 0$ from Equ.(3-15) we get,

$$V_{CE} = V_{CC}$$

Point B (0, V_{cc}/R_L):

When, $V_{CE} = 0$, again from the same equation we get,

$$I_C = \frac{V_{CC}}{R_L}$$

Now, if we put these points on the output characteristics of the transistor and connect them we get the load line as shown in Fig.3-18.

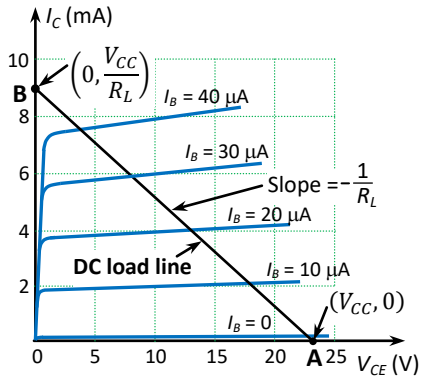


Fig.3-18: Load line drawn on the output characteristic curves

Equation (3-14) can be written as,

$$I_C = -\frac{1}{R_L}V_{CE} + \frac{V_{CC}}{R_L} \qquad (3\text{-}16)$$

Now, equation (3-16) is comparable with a standard equation of straight line,

$$y = mx + c \qquad (3\text{-}17)$$

Comparing equations (3-16) and (3-17) we find that, the slope of the load line is $-1/R_L$ and V_{CC}/R_L is the y-intercept. Thus, the shape of the load-line completely depends on the values of V_{CC} and R_L.

If the values of V_{CC} and R_L are fixed the operating point of the transistor can change only along this load line depending on the values of I_B. For example, if the value of I_B increases (with constant values of V_{CC} and R_L) the operating point will move toward the point *B* and if I_B decreases the operating point will move to point *A*. But, for a fixed value of I_B, the operating point also be fixed as shown in Fig.3-19.

Thus, the intersecting point of the *DC* load line and the output characteristic curve of a transistor is called the ***operating point***. It is also called the ***quiescent point*** or simply ***Q-point***. Therefore, a Q-point gives a fixed value of output voltage and output current which are represented as V_{CEQ} and I_{CQ}.

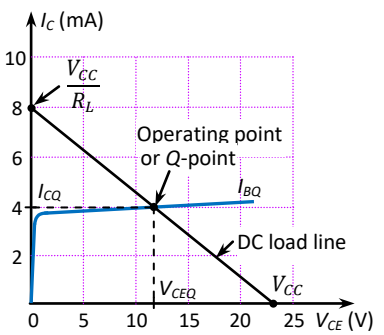


Fig.3-19: Operating point (intersection of load line and a fixed output characteristic curve).

3.9 Transistor Biasing Circuits

In Fig.3-17 we have seen how a transistor can be biased properly using a single voltage source (battery or power supply). This is the simplest form of biasing circuit. To achieve the fixed operating point, there are many other biasing circuits. The names of different biasing circuits are:

a) Fixed bias or base bias
b) Base bias with emitter feedback or emitter bias

c) Collector-to-base bias
d) Voltage divider bias

3.10 Fixed Bias Circuit

The simplest biasing circuit for transistor is the ***fixed bias*** which is shown in Fig.3-20(a). The collector resistor used in a transistor circuit is also called the load resistance. For biasing only a fixed resistance is used in the base circuit. That's why, this circuit is called ***fixed bias*** or ***base bias***. The value of the supply voltage and R_B sets a base current, I_B. Depending on the β of the transistor a collector current is developed. V_{CE} is determined by I_C, R_C and V_{CC}. The target of the biasing circuit is to set a DC operating point or bias point.

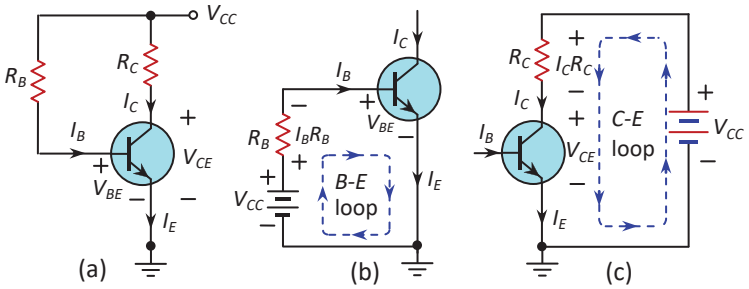


Fig.3-20: Fixed bias circuit, (a) Complete circuit, (b) *B-E* loop, and (c) *C-E* loop

Applying KVL in the base-emitter circuit [Fig.3-20(b)] we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$or, \quad I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad \boxed{I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}} \qquad (3\text{-}18)$$

Using this equation we can easily calculate the value of I_B. As, this value determines the position of *Q*-point, it is also represented by I_{BQ}.

If we know the value of β of the transistor, the collector current can be calculated as,

$$I_C = I_{CQ} = \beta I_B + I_{CEO}$$

But we know, $I_{CEO} = (\beta + 1) I_{CBO} \approx 0$.

$$\therefore \quad \boxed{I_C = I_{CQ} = \beta I_B + (\beta + 1) I_{CBO} \approx \beta I_B} \qquad (3\text{-}19)$$

Now, applying KVL in the collector-emitter circuit [Fig.3-20(c)] we get,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad \boxed{V_{CE} = V_{CEQ} = V_{CC} - I_C R_C} \qquad (3\text{-}20)$$

Using the equations (3-18) to (3-20), we can calculate the value of I_B, I_C and V_{CE} corresponding the operating point of the base bias circuit.

Example 3-2:

Assuming $V_{CC} = 12\ \text{V}$, $R_B = 180\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$ and a silicon transistor with $\beta = 100$, determine the operating point of the circuit of Fig.3-20(a). Sketch the load line and show the *Q*-point. Also calculate the saturation current considering $V_{CE(sat)} = 0.5\ \text{V}$.

Solution:

Using Equ.(3-18), the base current of the bias point is,

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{180\text{ k}\Omega} \approx 62.8\ \mu\text{A}$$

Using Equ.(3-19), collector current at the bias point is,

$$I_{CQ} = \beta I_B + (\beta + 1)I_{CBO} \approx \beta I_B = 100 \times (62.8\ \mu\text{A}) \approx 6.28\text{ mA [Ans.]}$$

Using Equ.(3.20), collector-emitter voltage at the operating point is,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12\text{ V} - (6.28\text{ mA}) \times (1\text{ k}\Omega) = 5.72\text{ V [Ans.]}$$

The calculated operating point and the load line is drawn in Fig.3-21.

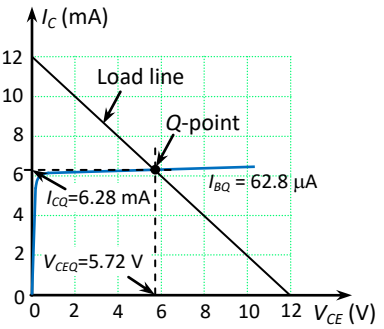


Fig.3-21: Load line and Q-point of example 3-2.

The saturation current can be calculated from Equ.(3-20) as,

$$V_{CEQ} = V_{CC} - I_C R_C \quad or, \quad 0.5\text{ V} = 12\text{ V} - I_C \times 1\text{ k}\Omega$$

$$\therefore\ I_C = \frac{12\text{ V} - 0.5\text{ V}}{1\text{ k}\Omega} = 11.5\text{ mA [Ans.]}$$

Comments: The load line and the operating point have been drawn using the method described in Section 3.8.

3.11 Fixed Bias with Emitter Feedback

This biasing circuit (also called ***emitter bias***) is exactly same as fixed bias, but an additional resistor (R_E) is used in the emitter terminal as shown in Fig.3-22(a). The function of R_E is to provide better stability of the DC operating point. The emitter resistor applies a voltage to the input circuit which is proportional to the output current. This mechanism is called ***feedback***. For this reason R_E is called emitter feedback resistor.

Calculation of Operating Point:

From the forward biased *B-E* circuit, using KVL [Fig.3-22(b)] we get,

$$V_{CC} - I_B R_B - V_{BE} - V_E = 0$$

$$or, \quad V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$or, \quad V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0\ [\because I_E = (\beta + 1)I_B]$$

$$or, \quad I_B[R_B + (\beta + 1)R_E] = V_{CC} - V_{BE}$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{3-21}$$

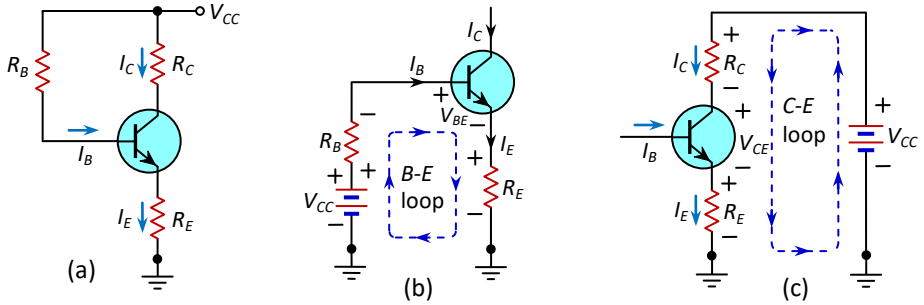


Fig.3-22: Fixed bias with emitter resistor, (a) Complete circuit, (b) *B-E* loop, and (c) *C-E* loop.

Once, I_B is found, the collector current can be calculated as,

$$I_C = \beta I_B + I_{CEO}$$

As the value of I_{CEO} is small, sometimes we neglect this leakage current. Then we can write,

$$\boxed{I_C \approx \beta I_B} \tag{3-22}$$

Now, applying KVL, in the *C-E* loop of Fig.3-22(c) we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$or, \quad V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \; [\because I_E \approx I_C]$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{3-23}$$

Using equations (3-21), (3-22) and (3-23), the operating point of the circuit can easily be calculated.

Stabilization Mechanism:

From the forward biased *B-E* circuit we have found,

$$V_{CC} - I_B R_B - V_{BE} - V_E = 0$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE} - R_E I_E}{R_B}} \tag{3-24}$$

For fixed values of V_{CC}, V_{BE}, and R_E the value of I_B will be fixed. Now, if due to the increase in temperature collector current I_C increases, I_E will also increase. Hence, according to Equ.(3-24), I_B will decrease. With this decrease in I_B, collector current I_C will decrease. In this way any attempt to increase I_C will automatically be adjusted. On the other hand, if I_C decrease from the DC bias point due to decrease in temperature, $I_E R_E$ will decrease, I_B will increase and I_C will also increase.

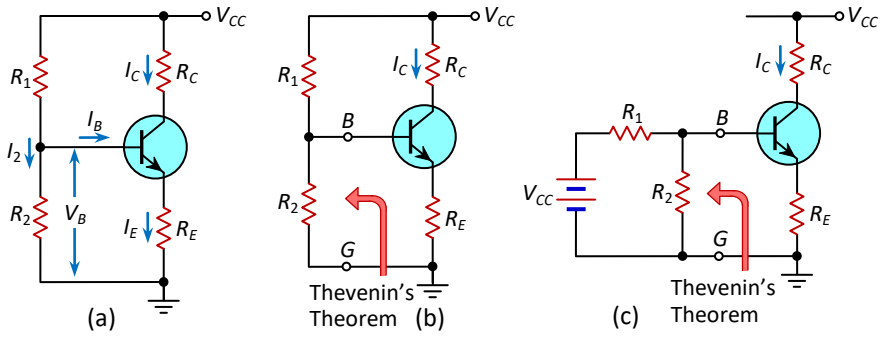


Fig.3-23: (a) Voltage divider bias circuit, (b) Location of Thevenin's theorem, (c) Fig. b is redrawn.

3.12 Voltage Divider Bias

Voltage divider biasing circuit, shown in Fig.3-23(a), is the best among all the biasing circuits. Here, V_{CC} is divided using a voltage divider network ($R_1 - R_2$) and then applied to base. For this reason, it is called ***voltage divider bias***. It is also called ***self bias***. By changing the ratio of R_1 and R_2 any value of voltage (V_B) can be set for the base circuit.

Calculation of the Operating point

The circuit can be analyzed in two methods: ***exact method*** and ***approximate method***. Exact method can be used for all voltage divider biasing circuit but not the approximate method. We will see the exact analysis method here.

First, we have to determine the Thevenin's equivalent circuit of the voltage divider portion, i.e., at the base-emitter terminals as shown in Fig.3-23(b) and 3-23(c).

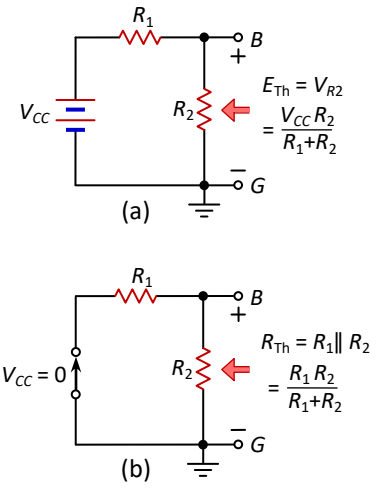


Fig.3.24: (a) Circuit for E_{Th} calculation, (b) Circuit for R_{Th} calculation.

E_{Th} Calculation: Thevenin's voltage will be the open circuit voltage across R_2 [see Fig.3-24(a)]. Applying voltage divider rule we get,

$$E_{Th} = V_{R2} = \frac{V_{CC}R_2}{R_1 + R_2} \tag{3-25}$$

R_{Th} Calculation: To calculate R_{Th}, first we have to replace the voltage source by short circuit as shown in Fig.3-24(b). Looking at the B and G terminals we find that R_1 and R_2 are in parallel. Therefore the Thevenin's resistance will be,

$$R_{Th} = R_1 \| R_2 = \frac{R_1R_2}{R_1 + R_2} \tag{3-26}$$

Now, if we redraw the biasing circuit using the Thevenin's equivalent, we get the circuit of Fig.3-25 (only the input loop is shown).

To calculate the value of I_B (which is also I_{BQ}), let us apply KVL in the base-emitter circuit of Fig.3-25.

$$E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E = 0 \qquad (3\text{-}27)$$

$$or, \quad E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - (\beta + 1) I_B R_E = 0 \; [\because I_E = (\beta + 1) I_B]$$

$$or, \; I_B [R_{\text{Th}} + (\beta + 1) R_E] = E_{\text{Th}} - V_{BE}$$

$$\therefore \quad \boxed{I_B = I_{BQ} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1) R_E}} \qquad (3\text{-}28)$$

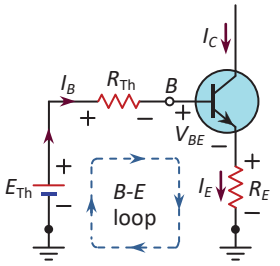


Fig.3-25: Base-emitter loop with Thevenin's equivalent circuit.

Therefore, the value of collector current will be,

$$\boxed{I_C = I_{CQ} = \beta I_B = \frac{\beta (E_{\text{Th}} - V_{BE})}{R_{\text{Th}} + (\beta + 1) R_E}} \qquad (3\text{-}29)$$

The collector-emitter loop will be exactly same as in the Fig.3-22(c). Applying KVL to that loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$or, \quad V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \; [\because I_E \approx I_C]$$

$$or, \quad V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$or, \quad \boxed{V_{CE} = V_{CEQ} = V_{CC} - I_C (R_C + R_E)} \qquad (3\text{-}30)$$

Using Equ.(3-28) to (3-30) the exact position of the operating point of voltage divider bias circuit can be calculated.

Example 3-3

For the voltage divider biasing circuit of Fig.3-26, calculate the following using exact analysis. (i) I_{BQ}, (ii) I_{CQ}, (iii) V_{CEQ}, (iv) V_E, and (v) V_{RC}.

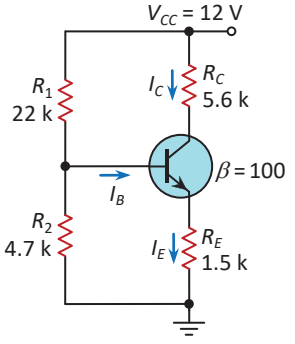


Fig.3-26: Voltage divider bias circuit for Example 3-3.

Solution:

Values of E_{Th} and R_{Th} can be calculated using Equ.(3-25) and Equ.(3-26) as,

$$E_{\text{Th}} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{12 \text{ V } (4.7 \text{ k}\Omega)}{(22 + 4.7) \text{ k}\Omega} \approx 2.11 \text{ V}$$

$$R_{\text{Th}} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(4.7 \text{ k}\Omega)\ (22 \text{ k}\Omega)}{(22 + 4.7) \text{ k}\Omega} \approx 3.87 \text{ k}\Omega$$

The biasing base current can be calculated using Equ.(3-28),

$$I_{BQ} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{2.11\ \text{V} - 0.7\ \text{V}}{3.87\ \text{k}\Omega + (100 + 1)1.5\ \text{k}\Omega} \approx 9.08\ \mu\text{A}\ [\text{Ans.}]$$

Now the quiescent collector current will be,

$$I_{CQ} = \beta I_B = 100 \times (9.08\ \mu\text{A}) = 0.908\ \text{mA}\ [\text{Ans.}]$$

Using Equ.(3-30), we can calculate V_{CEQ},

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 12\ \text{V} - 0.909\ \text{mA} \times (5.6\ \text{k}\Omega + 1.5\ \text{k}\Omega)\ \approx 5.55\ \text{V}\ [\text{Ans.}]$$

V_E and V_{RC} can be calculated multiplying R_E and R_C by the current flowing through them.

$$V_E = V_{RE} = R_E \times I_E \approx\ R_E \times I_{CQ} =\ 1.5\ \text{k}\Omega \times 0.908\ \text{mA} \approx 1.36\ \text{V}\ [\text{Ans.}]$$

$$V_{RC} =\ R_C \times I_{CQ} =\ 5.6\ \text{k}\Omega \times 0.908\ \text{mA} \approx 5.1\ \text{V}\ [\text{Ans.}]$$

Comments: As $V_{CEQ} \approx V_{RC}$ the operating point of the transistor will be at the middle of the load line which is a good design approach.

3.13 Transistor Modeling

To analyze transistor circuits, it is convenient to represent the transistor by its equivalent circuit. The process of representing a transistor by an equivalent circuit is called ***modeling***. There are different types of transistor modeling or equivalent circuits. Here, we will discuss only the r_e modeling. An NPN transistor circuit in common-emitter configuration is shown in Fig.3-27(a). Assume that the transistor is biased in the active region. We may consider this circuit as a four-terminal or a two-port network, keeping the emitter common to both the input and output port. Therefore, *B* and *E* will be in the input port, and the *C* and *E* will be in the output port. In a four-terminal network the directions of currents (i_i, and i_o) and the polarities of voltages (v_i, and v_o) are always as shown in this figure. Here, the parameters are written using lower-case letters to represent the AC values (e.g. i_e, i_b).

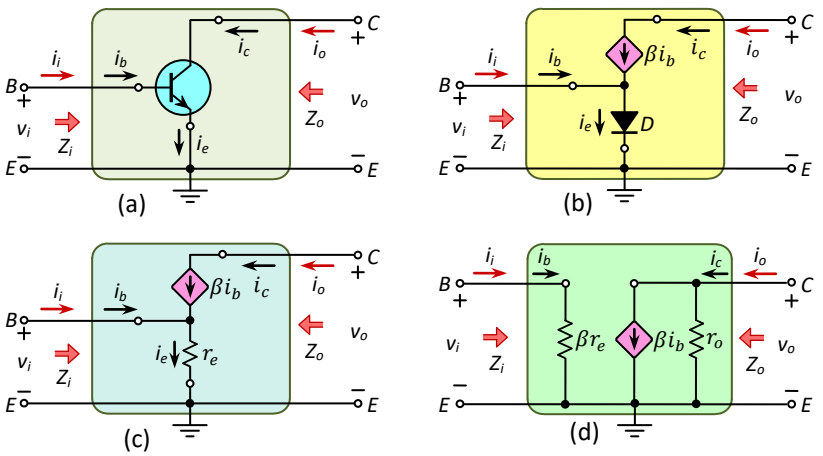


Fig.3-27:(a) NPN transistor in CEC, (b) Diode equivalent circuit, (c) Diode is replaced by r_e, and (d) r_e equivalent circuit

In a CE circuit, the input current (i_b) flows through a forward biased *B-E* junction, and due to the transistor action a large current flows through the collector terminal. The value of the

collector current is βi_b. We can consider the input side as a forward biased diode and the output side as a dependent current source whose value is $i_c = \beta i_b$. Thus, the transistor can be represented by a diode and a current source as in Fig.3-27(b). A forward biased diode after the knee point behaves like a resistor. So, the diode can be replaced by a resistor, which results in the circuit of Fig.3-27(c). Generally, these equivalent circuits are used for AC analysis. So, r_e is the AC resistance (or dynamic resistance) of the forward biased *B-E* junction and given by,

$$r_e = \frac{26\text{ mV}}{I_E} + r_B \approx \frac{26\text{ mV}}{I_E} \tag{3-31}$$

Here, r_B is the base spreading resistance. As the value of r_B is very small, it can be neglected. In calculating the value of r_e, the quiescent emitter current (I_{EQ}) is used.

Now, for the simplicity of calculation, we want to separate the input circuit from the output circuit. From the Fig.3-27(c), we can write,

$$v_i = i_e r_e = i_b(\beta + 1) r_e \approx i_b \beta r_e \tag{3-32}$$

From Equ.(3-32), we find that the emitter resistance r_e is reflected to the base circuit being multiplied by a factor $(\beta + 1)$. With this concept the circuit of Fig.3-27(c) can be drawn as in Fig.3-27(d). At the output circuit, we have to consider the output impedance (or resistance) that can be calculated as,

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \tag{3-33}$$

So by connecting r_o is parallel with the current source, the final equivalent circuit of a transistor in CE configuration is as shown in Fig.3-27(d).

3.14 Single-Stage Common-Emitter Amplifier

Common-emitter (CE) amplifier is mostly used in electronic circuits. CE amplifier has reasonably high voltage gain, moderate current gain, medium input impedance, and high output impedance. In addition to voltage amplification this amplifier produces $180°$ phase difference between the input and output signals. If we do not need phase-shift, we can eliminate it by cascading even number of CE amplifier stages.

A CE amplifier is shown in Fig.3-28 that shows the changes of voltage levels at different points of the amplifier. The input signal (v_s) is considered as a sinusoidal AC signal with very small peak-to-peak value. When this signal passes through the input-coupling capacitor (C_{ic}), it is superimposed with the base-voltage V_B. So the base-voltage changes in-phase with the input signal. When the input signal increases, the base-voltage also increases, and hence, the base current increases. Because of the increase in base-current, collector-current also increases ($\because i_c = \beta i_b$). When the collector-current increases, the voltage-drop across the collector-resistor (R_C) increases. Therefore, the voltage level at the collector terminal (that was initially V_{CQ}) decreases. As the output is taken from the collector, the output voltage decreases. The reverse process occurs when the input signal decreases. A small change in base current produces a very large change in collector current, and an amplified voltage is produced at the collector. The collector-voltage swings in the same frequency and shape of the input signal but $180°$ out off phase.

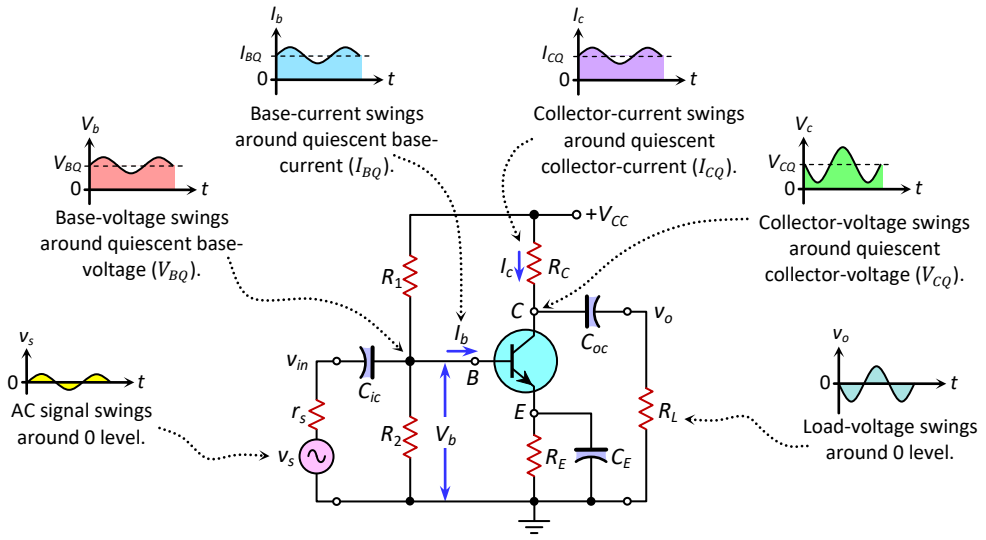


Fig.3-28: Waveforms of current and voltage swings at different points of CE amplifier

The amplified signal at the collector terminal has a DC voltage level as shown in Fig.3-28. When this signal passes through the output-coupling capacitor (C_{oc}), the capacitor blocks the DC voltage and the load resistor gets the pure amplified AC signal.

The voltage gain of this amplifier is given by

$$A_v = \frac{v_o}{v_{in}} = -\frac{(r_o \parallel R_C \parallel R_L)}{r_e} \qquad (3\text{-}34)$$

where, r_e = is the emitter resistance given by Equ.(3-31).
Generally, r_o (output resistance of the transistor) is very large and can be neglected.

$$\therefore A_v \approx -\frac{(R_C \parallel R_L)}{r_e} \qquad (3\text{-}35)$$

If R_L is not connected, i.e., considering $R_L = \infty$ $\quad \therefore \boxed{A_v \approx -\frac{R_C}{r_e}}$ (3-36)

Frequency Response of an Amplifier

The ***frequency response*** of any electronic device or system is the variation (if any) in the level of its output signal when the frequency of the input signal is changed. In other words, ***frequency response*** is the manner in which the device or the system responds to the change of frequency of input signal. The output voltage and, hence, the gain of an amplifier decreases for very low and for very high frequency of input signal, even, if the amplitude of the input remains same. This situation is illustrated in Fig.3-29. In this figure, the amplitude of the input signal is same for three cases, but the frequency has been changed. In the first case [Fig.3-29 (a)], the frequency of the input signal is very low and hence the amplitude of the output signal is lower than that of input signal. It means that the input signal has been attenuated at the output, due to its very low frequency. Similarly, the input signal has been attenuated at the output due to very high

frequency as shown in Fig.3-29(c). On the other hand, in Fig.3-29(b) the input signal has medium frequency and, therefore, has been properly amplified at the output.

Although here the cases of three discrete frequencies have been explained, the gain of the amplifier increases gradually with the increase in frequency. At the medium frequency range the amplifier gives the maximum gain. Again for higher frequencies, the gain of the amplifier falls gradually. This situation is illustrated in Fig.3-30. The graph shows the change of gain of the amplifier with the change in frequency. This graph is called the ***frequency response*** of an amplifier.

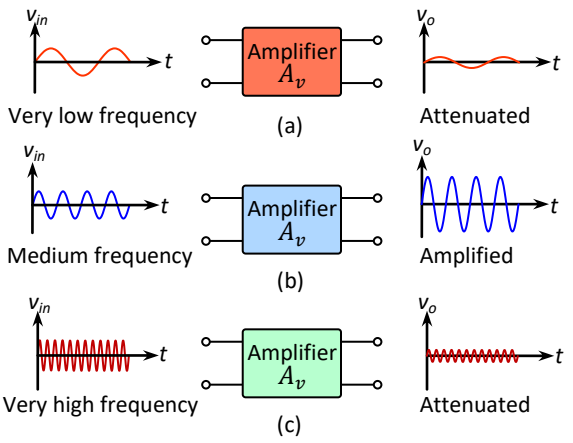


Fig.3-29: Response of an amplifier to different frequency-inputs

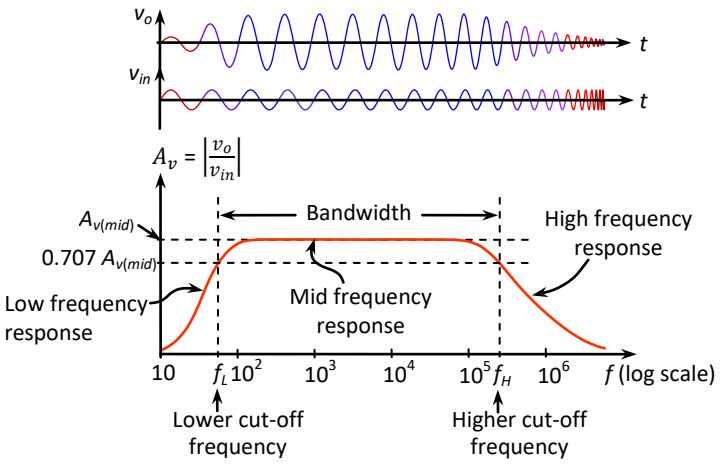


Fig.3-30: Frequency response of a typical amplifier

Phase Response

The ***phase response*** of any electronic device or system is the variation phase angle of its output signal when the frequency of the input signal is changed. Variation of the level (amplitude, or RMS value) of the output signal is usually accomplished by a variation in the phase angle of the output relative to the input signal. Due to the page limitation, the phase response has not been discussed here.

3.15 Transistor as a Switch

BJT may be used as an amplifier or as a switch. To use the transistors as amplifier the operating point is set in the active region. But to use as a ***switch***, the transistor is biased in such a way that it can operate either in the cutoff region (OFF switch) or in the saturation region (ON switch). Fig.3-31 shows how a transistor can be used as a switch. The controlling voltage V_i will drive the switch ON/OFF. Here, the collector resistor, R_C, works as the load for the switch. In our home, we use manual switch, but the transistor is a voltage controlled switch. Hence, it can be drived by some other controlling circuits (such as a microcontroller based circuit).

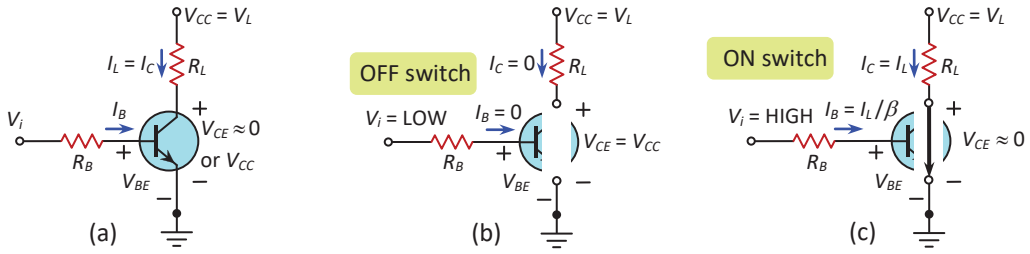


Fig.3-31: Switching action of transistor (a) Switching circuit, (b) Transistor is open (OFF), and (c) Transistor is closed (ON).

When the driving voltage is high (greater that 1 V), the *B-E* junction will be forward biased and current will flow through the load. The transistor will be saturated, i.e., the value of V_{CE} will be minimum ($V_{CE(sat)} \approx 0.2\,V$) and the transistor will work as an ***ON switch***. Almost the full supply voltage (V_{CC}) will be dropped across the load. But if the driving system provides low voltage (less than 0.5 V), the *B-E* junction will not be forward biased, and hence, the transistor will work as ***OFF switch*** and only the leakage current I_{CEO} will flow through the load. Almost the full supply voltage will be dropped across the transistor, i.e., $V_{CE} = V_{CC}$. As the current is almost zero, the load will not get power. When used as switch, the transistor operates either in saturation or cutoff region as shown in Fig.3-32.

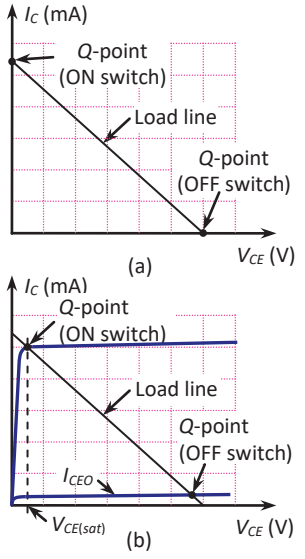


Fig.3-32: Load line of transistor switch (a) Ideal transistor, and (b) Practical transistor

3.16 Practical Transistors

In the market a lot of transistors are available with different sizes and shapes. All of them have different specifications.

Fig.3-33: Photographs of different transistors

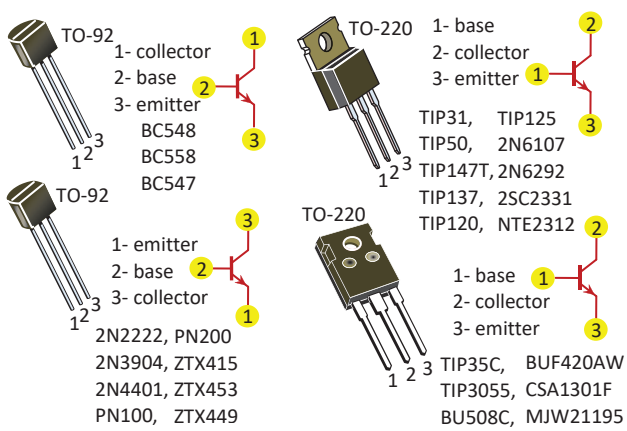


Fig.3-34 : Pin diagrams of some common transistors

Some are for low power and some are for high power. Some transistors have large bandwidth and some have low bandwidth. Though, the detailed discussion of them is out of scope of this souvenir, the photographs of some very common transistors are shown in Fig.3-33. On the other hand, Fig.3-34 shows the terminal names of some common transistors.

3.17 Transistor Testing Using Multimeter

Transistor can be tested (whether good or damaged) using a multimeter by measuring h_{FE} $(= \beta)$. The transistor has to be removed from the circuit and placed on the h_{FE} measuring slot as shown in Fig.3-35. The multimeter has eight connecting holes for this purpose. Four holes are for NPN transistor, and four holes for PNP transistor. The transistor has to be inserted into the appropriate holes, i.e., the B, E, C terminals of the transistor must be inserted into the B, E, C holes of the multimeter, respectively. The multimeter must show the value of β (or h_{FE}) of the transistor if it is OK. If the multimeter displays 'OL', instead of showing the value of β (h_{FE}), then the transistor is not operational.

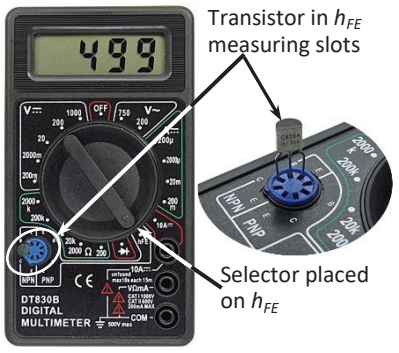
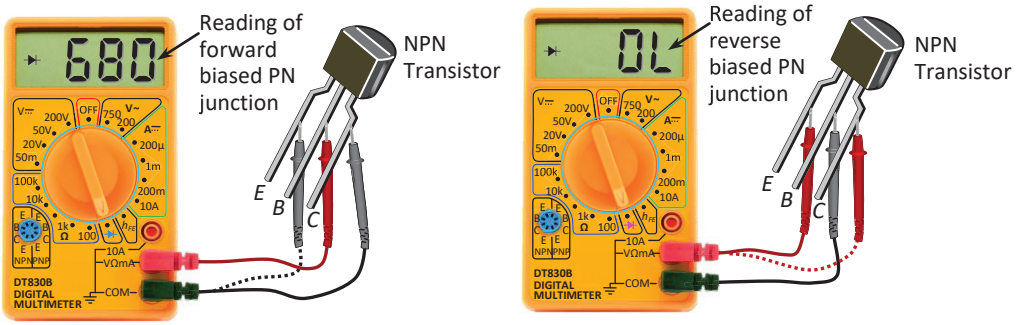


Fig.3-35 : Transistor testing using multimeter

On the other hand, if the multimeter has no β (h_{FE}) measuring facility, a transistor can be tested by measuring the PN junctions between *E-B* and *B-C* terminals. If the transistor is OK, the forward biased PN junction should give the reading of the barrier voltage as shown in Fig.3-36(a). On the other hand, the reverse biased PN junction should give high resistance ('OL') reading as shown in Fig.3-36(b). A damaged (internally opened) transistor may show 'OL' in both forward biased and reverse biased conditions (not shown in the figure). A damaged (internally shorted) transistor may show '0 V' in both forward biased and reverse biased conditions.



(a) *E-B* and *C-B* PN junctions are forward biased

(b) *E-B* and *C-B* PN junctions are reverse biased

Fig.3-36: Transistor testing using multimeter

CHAPTER

4

Field Effect Transistor (FET)

4.1 Introduction

The main problem of BJTs is their low input resistance. The solution of this problem is another device called ***Field-Effect Transistor*** or FET. While BJT is a current-controlled device, FET is a voltage-controlled device. The controlling voltage (input voltage) does not produce any current but an electric field to control the output current. As the output current is controlled by the electric field, the device is called the ***Field-Effect Transistor*** (FET).

4.2 Comparison of FET with BJT

Both BJTs and FETs can be employed as amplifiers and switches. The comparisons of BJTs and FETs are given in Table 4.1.

Table: 4.1 Comparison of FET and BJT

FET	BJT
• FET is a unipolar semiconductor device because its operation depends upon the flow of only majority carriers, i.e., either holes or electrons.	• BJT is a bipolar semiconductor device because both the majority carriers and minority carriers of the device constitute the current.
• The input impedance of FET is much larger than that of BJT.	• The input impedance of BJT is very lower than that of FET.

• FET is a voltage-controlled device.	• BJT is a current-controlled device.
• FET has higher frequency response, i.e., it can work with higher frequencies.	• BJT has comparatively lower frequency response, i.e., it cannot work with higher frequencies.
• FET provides better thermal stability because of the absence of minority carriers.	• Due to the minority carriers BJT provides less thermal stability: if not properly controlled, thermal damage may occur.
• The relationship between input and output quantities is nonlinear.	• The relationship between input and output quantities is almost linear.
• FET has small gain-bandwidth product.	• BJT has higher gain-bandwidth product.
• Switching speed of FET is high.	• Switching speed of BJT is low.
• FET is generally costlier than BJT.	• BJT is relatively cheaper than FET.

4.3 Classification of FET

Although there are many types of Field-Effect Transistors, two of them are most commonly used. These are ***Junction Field-Effect Transistors*** (JFET) and ***Metal-Oxide-Semiconductor Field-Effect Transistor*** (MOSFET). According to their construction and types of semiconductor materials used for fabrication, they are further classified into different types. The classification of Field-Effect Transistors with their names and symbols is given in the following tree (Fig.4-1).

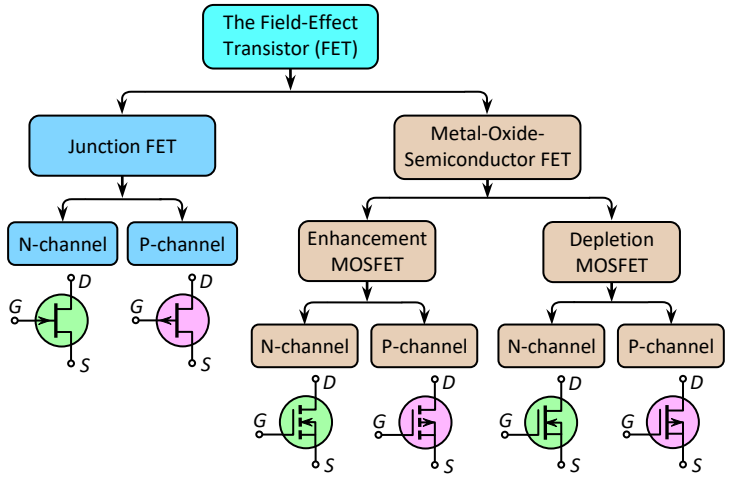


Fig.4-1: Different types of field-effect transistors

4.4 Construction of Junction Field-Effect Transistor (JFET)

Like the BJTs, field-effect transistors are also three-terminal device. The names of the terminals are: ***Drain*** (*D*), ***Source*** (*S*) and ***Gate*** (*G*). As shown in Fig.4-2, the construction of a FET may starts from an N-type or a P-type semiconductor bar. Let us start with an N-type semiconductor bar. On both opposite sides of the N-type materials, two P-type semiconductors are embedded. Metal

contacts are given to these P-type materials and are internally shorted together. This common terminal behaves as the ***Gate***(*G*) of the device. Similarly, two metal contacts are produced on the

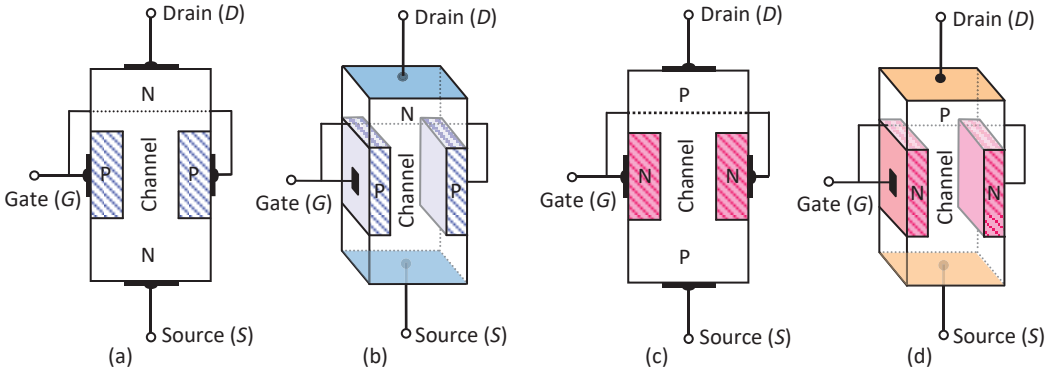


Fig.4-2: Construction of JFET: (a), (b) N-channel and (c), (d) P-channel.

two opposite ends of the N-type semiconductor. One of them is called the ***Drain*** (*D*) and the other is called the ***Source*** (*S*). The region of N-type material between the two P-type regions is called the ***channel***. Since, the channel is N-type semiconductor, this type of structure is called ***N-channel Junction Field-Effect Transistor***. On the other hand, if the starting semiconductor is P-type and two N-type semiconductors are embedded in the opposite faces, the resultant device is called the ***P-channel*** JFET [Fig.4-2(a and c)].

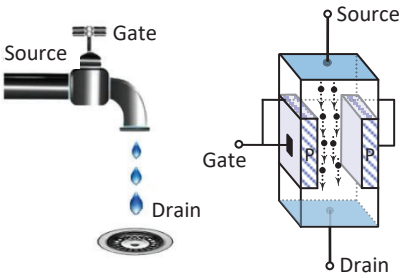


Fig.4-3: Water-tap analogy of FET

An analogy called ***water-tap analogy*** helps to understand the function of the terminals of a FET. As shown in Fig.4-3, water falls to the drain from source. The flow of water can be controlled by the key of the tap, which is equivalent to the gate of the FET. In a FET, electrons flow from the source to the drain. The flow of electrons can be controlled by the gate.

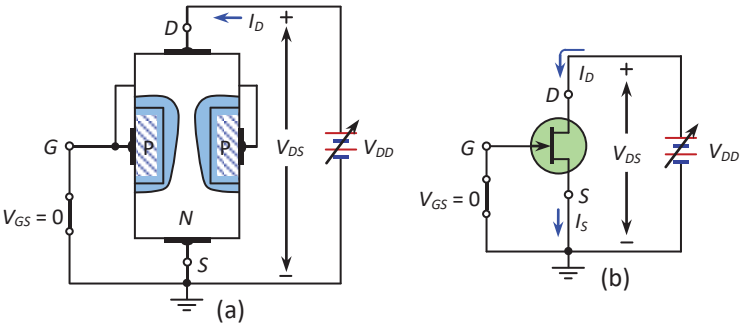


Fig.4-4: Biasing circuit of an N-channel JFET: (a) Block diagram, and (b) Schematic diagram

4.5 Operation of Junction Field-Effect Transistor (JFET)

Here, the operation of an N-channel JFET is explained. The operation process of the P-channel JFET will be same but the polarity of the biasing voltage, and the direction of current will be

opposite. The drain of an N-channel JFET has to be connected to higher potential and the source to the lower potential as in Fig.4-4 (i.e., $V_{DS} > 0$ V). The gate terminal is never forward biased. It is either reverse biased ($V_{GS} < 0$ V) or connected to ground ($V_{GS} = 0$ V). Therefore, the operation of JFET will be explained for two conditions.

$V_{GS} = 0$ V and $V_{DS} > 0$ V

For proper biasing of N-channel JFET, a potential difference V_{DS} is established by connecting the positive terminal of an external voltage source (V_{DD}) to drain, and the negative terminal to ground. The source terminal (*S*) is connected to ground. To make $V_{GS} = 0$, gate terminal (*G*) is also connected to ground as shown in Fig.4-4. As there exists a continuous N-type channel between the drain and source, electrons flow from source to drain, and the conventional current flows from drain to source and is limited by the resistance of the channel. This current is denoted as I_D. The junctions between the P-type gates and the N-type channel will be reverse biased as P-type gates are connected to ground. To understand this, let us represent the continuous resistance of the channel by three equal discrete resistors as shown in Fig.4-5. The potential at point A will be positive with respect to ground and its value will be $\frac{1}{3}V_{DS}$. As the gates are connected to ground, the $\frac{1}{3}V_{DS}$ voltage will reverse biase the PN junction between the P-type gates and N-type channel. As the N-channel is lightly doped and P-type gates are highly doped, the width of the depletion layer will increase more in the channel than in the gates. The potential at point B will be $\frac{2}{3}V_{DS}$. Therefore, the PN junction at pint B will be reverse biased by $\frac{2}{3}V_{DS}$. In this way, the reverse bias voltage will gradually increase from source to drain. So, the width of the depletion layer will be higher at the drain side than the source side. Thus, the depletion layer in the channel will achieve a shave called ***wedge shape***, as shown in Fig.4-5.

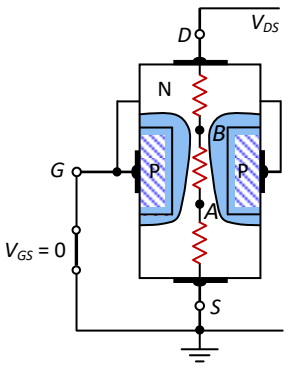


Fig.4-5: V_{DS} is distributed along the resistance of channel

Now if the value of V_{DS} is increased gradually, the reverse bias of the PN junctions increase and the width of the depletion layers also increase. Thus, the cross-sectional area of the channel decreases. With the decrease of cross-sectional area, the resistance of the channel increases. Therefore, with the increase in V_{DS}, I_D increases, but the rate of change will decrease due to the increase of resistance.

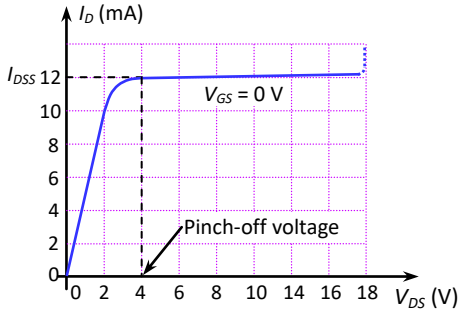


Fig.4-6: Variation of I_D with V_{DS} (Output characteristics)

If we go on increasing V_{DS}, the width of the depletion regions in the channel will be so large that, they will almost touch each other at a point near the drain end. This situation is called ***pinch-off***,

as shown in Fig.4-7. The value of V_{DS} for which pinch-off occurs is called the ***pinch-off voltage, V_P***. If the value of V_{DS} is increased further beyond $|V_P|$, drain current I_D does not increase. The maximum drain current produced at $V_{DS} = |V_P|$ with $V_{GS} = 0$ is called ***Drain-to-Source Saturation*** current and is denoted as I_{DSS}.

Therefore, keeping $V_{GS} = 0$, if we gradually increase V_{DS}, I_D increases up to $V_{DS} = |V_P|$. At this point the drain current is maximum which is I_{DSS}. If V_{DS} is increased further the drain current remains constant at I_{DSS}. The variation of I_D with V_{DS} is shown in the graph of Fig.4-6.

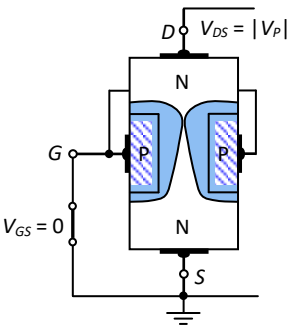


Fig.4-7: Pinch-off occurs when $\boldsymbol{V_{DS} = V_P}$.

$V_{GS} < 0$ V and $V_{DS} > 0$ V

If a small negative voltage is applied between the gate and source, say $V_{GS} = -1$ V, the gate-channel PN junction will be initially reverse biased and the channel width will reduce. Now, if V_{DS} is gradually increased, I_D will also increase. But, as the width of the channel is lower than that for $V_{GS} = 0$ V, pinch-off will occur for lower values of V_{DS} and the maximum drain current will be lower than I_{DSS}. In fact, now, pinch-off will occur at $V_{DS} = |V_P| - 1$V. If V_{DS} is increased further (beyond $|V_P| - 1$ V), drain current will remain constant as before. The output characteristic curve for this situation is shown in Fig.4-8.

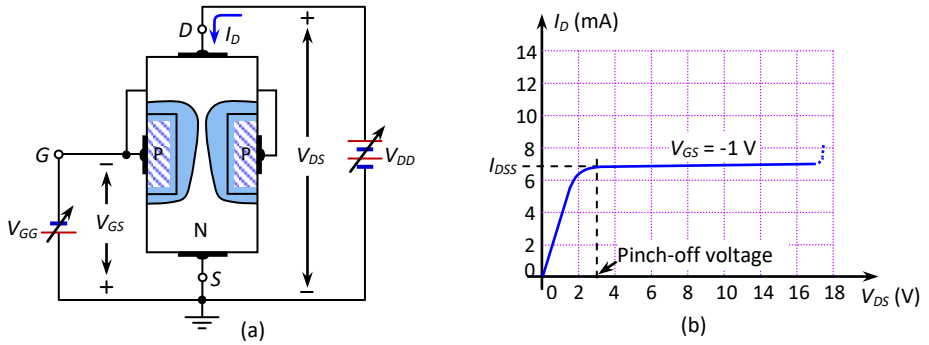


Fig.4-8: Operation of JFET for $\boldsymbol{V_{GS} < 0}$V: (a) Biasing circuit, and (b) Output characteristic curve

If the procedure, we have just described, is repeated with $V_{GS} = -2$ V, and $V_{GS} = -3$ V etc., we will find the graphs of same shape but lower values of drain current. Now pinch-off will occur at $V_{DS} = |V_P| - 2$ V and $V_{DS} = |V_P| - 3$ V, respectively. Finally, if we set $V_{GS} = -V_P$, pinch-off will occur at $V_{DS} = |V_P| - V_P = 0$ V. Due to this pinch-off at $V_{DS} = 0$ V, the device will be completely OFF and no drain current will flow. This value of gate-source voltage for which the device is cut-off, is called ***gate-to-source cutoff voltage*** and denoted by $V_{GS(cutoff)}$. In fact, $V_{GS(cutoff)} = V_P$.

If the pinch-off points of different output curves are joined together, we will get a parabola as shown by the dashed line in the output characteristic curves. The values of V_{DS} on this parabola are called ***drain-source saturation voltage***, $V_{DS(sat)}$. At any value of V_{GS}, the corresponding

value of $V_{DS(sat)}$ is the difference between V_{GS} and V_P, i.e., $V_{DS(sat)} = |V_P| - |V_{GS}|$. The shape of the parabola is determined by the constants I_{DSS} and V_P and is given by the following equation:

$$I_D = I_{DSS}\left(\frac{V_{DS(sat)}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (4\text{-}1)$$

4.5.1 Output Characteristics

In any field-effect transistor (for common-source configuration), the drain current, I_D is the output current and the drain-source voltage V_{DS} is the output voltage. The gate-source voltage, V_{GS} is the input voltage. Being the voltage-controlled device, the input current of FET is negligibly small. Therefore, the $I_D - V_{DS}$ characteristic curves described in the operation of JFET are the output characteristics. A set of output characteristic curves is shown in Fig.4-9(b). The region between the y-axis and the parabola is called the ***voltage-controlled resistance*** region or ***ohmic region***. In this region, the channel-resistance is controlled by V_{GS} as we have found before. Here, the output current, I_D, increases with the increase in output voltage (V_{DS}) for a fixed value of $V_{GS} \leq 0\,V$. The intersecting point of any output curve with the parabola is called the saturation voltage $V_{DS(sat)}$. The region on the right of the parabola is called the ***active region*** or ***pinch-off region***. In this region, I_D remains almost constant though the output voltage V_{DS} is increased. This is the region where a FET works as an amplifier.

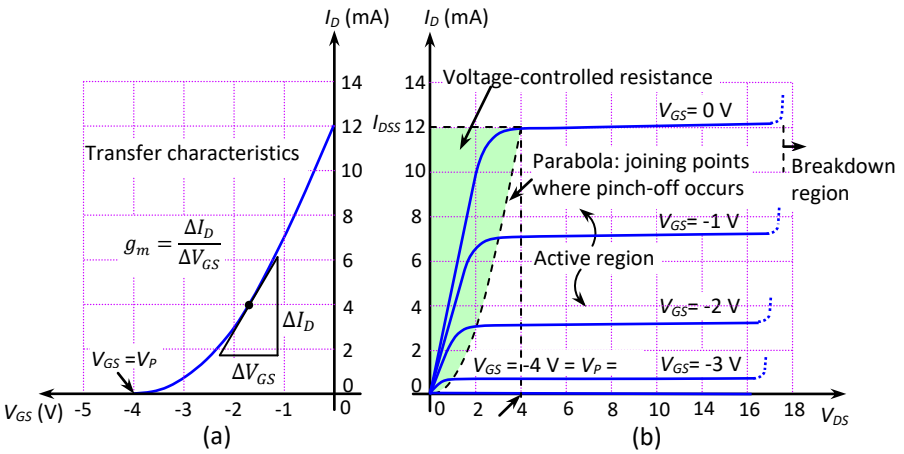


Fig.4-9: (a) Transfer characteristic curve, and (b) Set of output characteristic curves

If V_{DS} is increased beyond the tolerance level of the device, channel breakdown occurs and I_D increases abruptly. In JFET, breakdown is caused by the avalanche mechanism, described in PN junction chapter. Note that the larger the magnitude of $|V_{GS}|$, the smaller the value of V_{DS} at which breakdown occurs [shown in Fig.4-9(b)].

The relation between the input voltage and output current is given by

$$I_D = I_{DSS}\left(\frac{V_{DS(sat)}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (4\text{-}2)$$

4.5.2 Transfer Characteristic

In JFET the output current (I_D) is controlled by the input voltage. The relationship between the input voltage, V_{GS} and the output current, I_D (for common source configuration) for a fixed value of $V_{DS} > |V_P|$ is called the ***transfer characteristic curve***. The shape of transfer characteristic curve is also determined by the values of V_P and I_{DSS}.

Fig.4-10 shows a transfer characteristic curve of an N-channel JFET that has $V_P = -4\,\text{V}$ and $I_{DSS} = 12\,\text{mA}$. From this graph, it is clear that, by increasing the reverse bias voltage of the gate the output current can be decreased. When $V_{GS} = 0\,\text{V}$, the drain current is maximum (I_{DSS}) and when $V_{GS} = V_P$, the output current becomes zero. The relationship between the input voltage and the output current is not liner, and this relationship is given by an empirical formula called ***Shockley's equation***. In fact, this equation is same as the equation of the parabola of output characteristics. The Shockley's equation is,

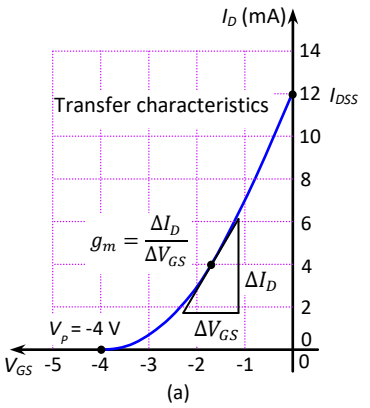


Fig.4-10: Transfer characteristic curve

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (4\text{-}3)$$

Here, I_{DSS} and V_P are constants for a particular JFET, output current I_D is the controlled variable and the input voltage V_{GS} is the controlling voltage.

The slope of the curve at any point is called ***trans-conductance***, g_m and can be measured as,

$$g_m = \frac{i_d}{v_{gs}} = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}=\text{constant}} \quad (\text{S or } \mho) \qquad (4\text{-}4)$$

The value of g_m is high at the upper portion of the curve and its value is less at the lower portion of the curve.

4.6 JFET Biasing Circuits

Like the BJT biasing circuits, there are many biasing circuits for FETs. Here, only self-biasing circuit is discussed. This biasing circuit is comparatively better than fixed-bias circuit. The self-bias circuit for common-source configuration of N-channel JFET is shown in Fig.4-11. The drain is connected to the positive terminal via the load resistance R_D, and source is connected to ground through R_S. The gate is connected to ground with a resistor R_G. The gate resistor R_G has no effect in the biasing condition, but this resistor helps the input signal to be applied at the gate terminal. The reverse bias of the gate

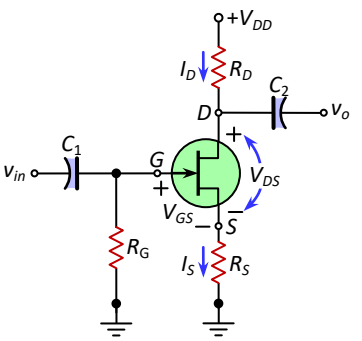


Fig.4-11: Self-bias for common-source JFET

terminal is established by the voltage drop across the source resistor R_S.

Calculation of Operating Point:

Applying KVL in the input circuit (gate-source of Fig.4-12(a)) we get,

$$+I_G R_G - V_{GS} - I_S R_S = 0$$

$$+I_G R_G - V_{GS} - I_D R_S = 0 \; [\because I_D = I_S]$$

But for any FET the value of gate current is approximately zero. That is $I_G = 0$. Therefore,

$$V_{GS} = -I_D R_S \tag{4-5}$$

Now putting this value into the Shockley's equation we get,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{|I_D R_S|}{|V_P|}\right)^2 \tag{4-6}$$

Equ.(4-6) contains only one variable I_D and some constants. So, solving this equation we can find the value of I_D. Being a quadratic equation, it will be little difficult to solve this equation. In that case we can use the graphical method to solve this equation.

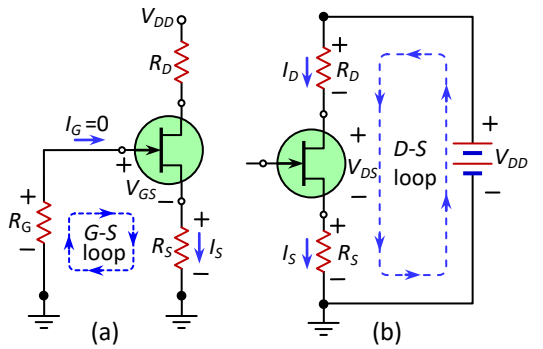


Fig.4-12: Input and output loops of self-bias circuit

Again, applying KVL in the output (drain-source) circuit, we get,

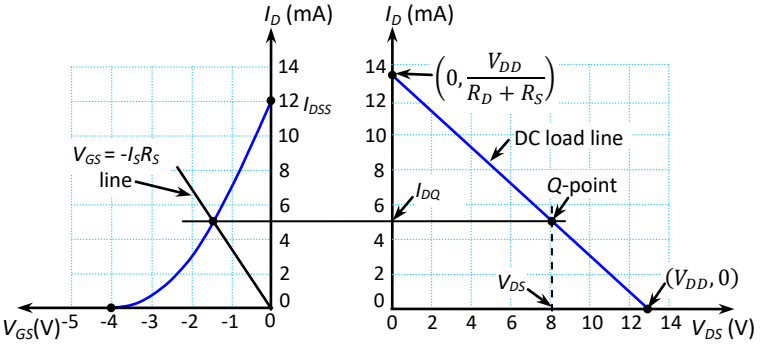
$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\because I_D = I_S, \; \therefore V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{4-7}$$

Using Equ.(4-7) and Equ.(4-6), the DC operating point of a fixed bias circuit can be determined. The last equation is also used to draw the load line.

Determination of Operating Point Using Graphical Method

Without solving the equations [Equ.(4-6)], we can determine the position of operating point graphically. For this purpose, we have to draw the transfer characteristics using Equ.(4-3). On the transfer characteristic curve, we have to draw the bias line given by Eq.(4-5) as shown in Fig.4-13. The intersecting point of this bias line with the transfer characteristic curve will give



(a) Bias line on transfer characteristics (b) Operating point on load line

Fig.4-13: Determination of operating point using graphical method

the value of quiescent drain current I_{DQ}. After determining the value of I_{DQ}, the value of V_{DSQ} can be calculated using Equ.(4-7) or using the graph. We have to draw the load line and a horizontal line through the intersecting point on the transfer characteristics. This horizontal line will intersect the load line and the abscissa of this point is the value of V_{DSQ}. In fact, this point is the DC biasing point of the FET circuit.

4.7 FET Pin-Diagrams

Like the BJTs, FETs are manufactured with different packages. The pin diagrams vary from package to package. Some very common packages of FETs with their pin-diagrams are shown in Fig.4-14.

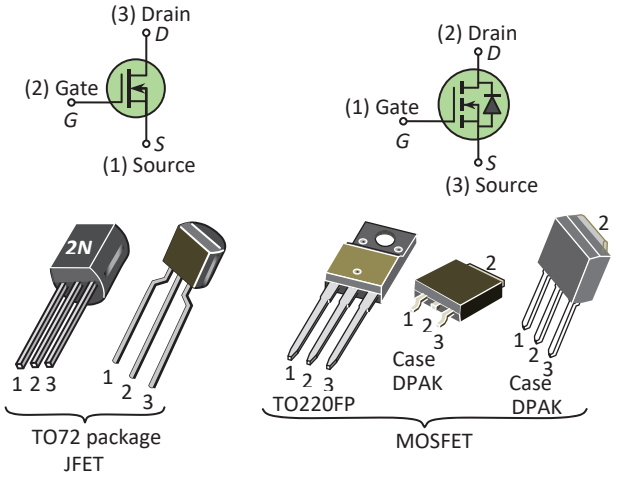
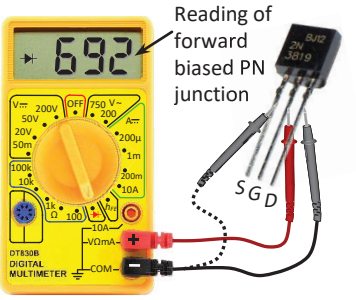


Fig.4-14: Pin-diagrams of some common FETs

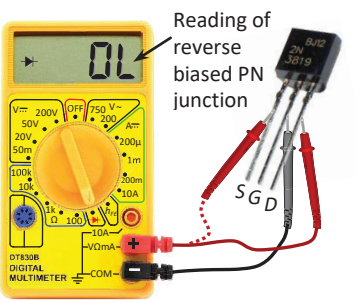
4.8 Testing Procedure of FETs

Like BJTs and diodes, we can check field-effect transistors (FETs) using multimeter. As shown in Fig.4-2, there are two PN junctions between gate-drain, and gate-source terminals. In section 2-17, we discussed how a PN junction can be tested using multimeter. We can apply the same process to test the PN junctions of a JFET. As shown in Fig.4-15, the selector of the multimeter has to be set on 'Diode Testing Position'. If the junctions are forward biased, the meter reads the barrier voltage [Fig.4-15(a)]. But if the junctions are reverse biased, the meter will show 'OL' (over load) [Fig.4-15(b)]. These are the indications of a good JFET. A faulty JFET will give different readings.

Using the diode testing process, we cannot test a MOSFET, because the gate (*G*) is completely isolated from channel (discussed later). However, using resistance measurement, we can test if the gate terminal is short or if the drain and source terminals are open or short. For resistance measurement, the selector has to be placed on '100 kΩ' position. The resistance between *G-S*, and *G-D* should very high. If the meter shows low resistance (0 or few ohms), the gate terminal is shorted. A good DMOSFET will show finite resistance between drain and source, and a good EMOSFET should show very high resistance between drain and source.



(a) *G-S* and *G-D* PN junctions are forward biased



(b) *G-S* and *G-D* PN junctions are reverse biased

Fig.4-15: JFET testing using multimeter

4.9 Single Stage Common Source Amplifier

Like the BJT CE amplifiers, FET common-source (CS) amplifiers are mostly used. CS amplifier has voltage gain (though less than BJT amplifiers), high current gain, high input impedance, and high output impedance. Due to its high input impedance, CS amplifiers are generally used at the first stage of electronic systems. Like a CE amplifier CS amplifier also produces 180° phase difference between the input and output signals.

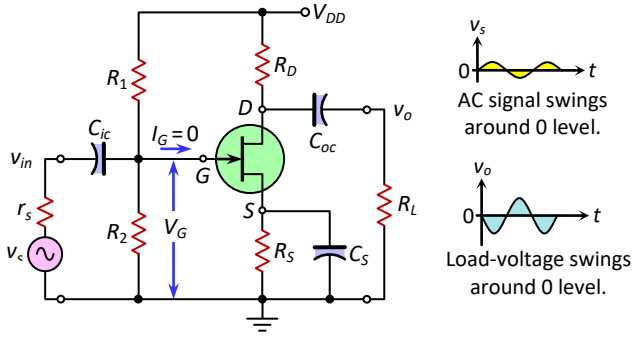


Fig. 4-16: FET Common source amplifier circuit

Fig.4-16 shows a CS amplifier using voltage divider bias. The changes of voltage and current levels at different points (as shown in Fig.4-17) of this amplifier will be exactly same as for CE amplifier. The input AC signal (v_s) has a very small peak-to-peak value. When this signal passes through the input-coupling capacitor (C_{ic}), it superimposes with the DC gate-voltage V_G. So the gate-voltage changes in-phase with the input

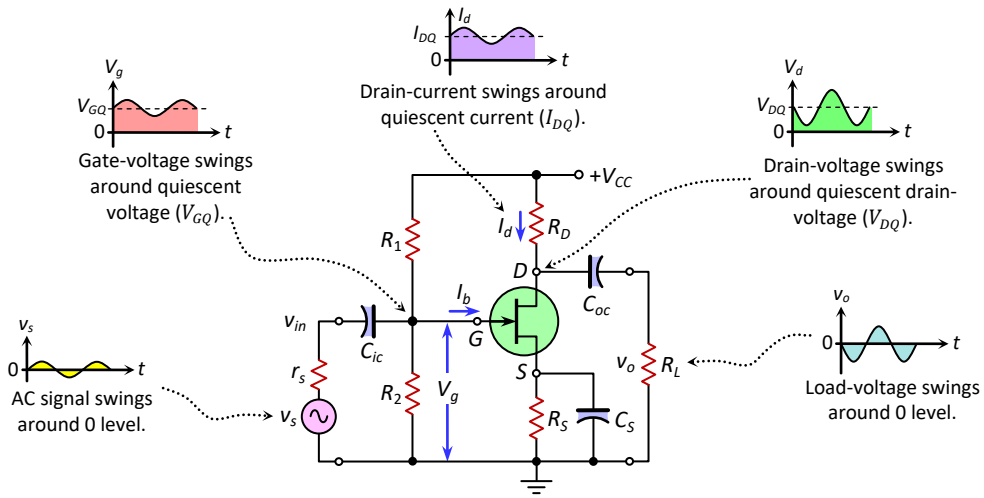


Fig.4-17: Waveforms of current and voltage swings at different points of CS amplifier

signal. When the input signal increases, the drain-current also increases ($\because I_d = g_m v_{gs}$). When drain-current increases, the voltage-drop across the drain-resistor (R_D) increases. Therefore, the voltage level at the drain terminal (that was initially V_{DQ}) decreases. As the output is taken from the drain, the output voltage decreases. The reverse process occurs when the input signal decreases (negative half-cycles). A small change in input voltage produces a large change in drain current that flow through a large resistor, R_D. So, an amplified voltage is produced at the collector. The drain-voltage swings with the same frequency and shape of the input signal but 180° out off phase.

The amplified signal at the drain terminal has a DC voltage level as shown in Fig.4-17. When this signal passes through the output-coupling capacitor (C_{oc}), the capacitor blocks the DC voltage and the load resistor gets the pure amplified AC signal.

4.10 Metal-Oxide-Semiconductor FET (MOSFET)

Metal-oxide-semiconductor FET (MOSFET) is similar, in many respects, to JFET. Both of them have drain, source, gate and channel and both of them work by controlling the channel resistance applying a gate-to-source voltage. The main feature that distinguishes a MOSFET from a JFET is that the gate terminal in a MOSFET is insulated from its channel region. So, they provide very large input impedance. There are two types of MOFSFETs: ***Depletion*** MOSFET or **DMOSFET** and ***Enhancement*** MOSFET or **EMOSFET**.

4.11 Construction of MOSFET

Like the JFETs, there are two types of MOSFETs: ***N-channel*** MOSFET and ***P-channel*** MOSFET. Construction of N-channel MOSFET starts from a block of lightly doped (low conductivity) P-type semiconductor called ***substrate***. Into the substrate, two heavily doped N-type regions are constructed (diffused) as shown in Fig.4-18. One of them works as drain and the other as source. A thin (not more than 1000 Å) layer of silicon dioxide (SiO_2) is deposited along the surface where the N-type drain and source have been made. Using photo-lithography and etching, two holes are made through the oxide layer over the drain and source. Through these holes, two metal contacts are given to the N-type materials, that work as the drain and source terminals. Now metal (aluminum) is deposited on SiO_2 layer in between the drain and source. This contact is the gate terminal of the device. Another metal contact is also made to the substrate on the opposite surface. In most of the devices, this substrate terminal is internally connected to source terminal.

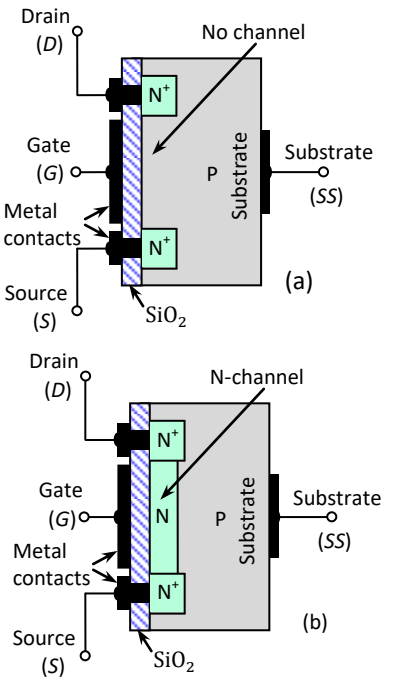


Fig.4-18: Construction of N-channel MOSFET: (a) Enhancement, and (b) Depletion

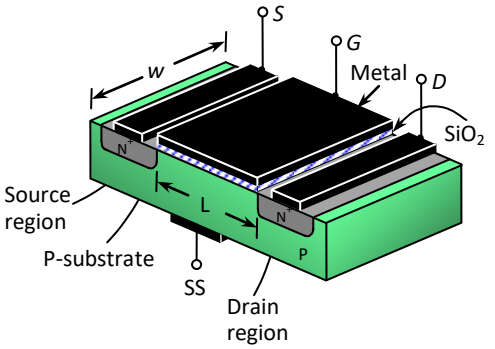


Fig.4-19: Construction of N-channel enhancement MOSFET (3-D view)

The MOSFET structure constructed so far [Fig.4-18(a)] has P-type material in between the drain and source, that is, there is no continuous path between the drain and source. This type of MOSFET is called the ***enhancement*** MOSFET. However, if an N-type channel is made between drain and source during the diffusion process, the structure is called ***depletion*** MOSFET [Fig.4-18(b)]. Depletion MOSFET has a ready channel from drain to source but in enhancement MOSFET there is no ready channel between the drain and source. The construction of MOSFET transistor is further illustrated in a three-dimensional structure in Fig.4-19.

Construction of P-channel MOSFETs is same (Fig.4-20). Here, construction starts from a lightly doped N-type material on which highly doped P-type drain, source and channel (for enhancement device) are made.

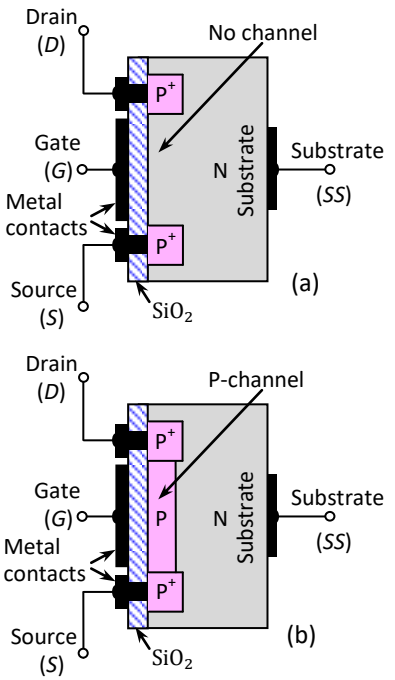


Fig.4-20: Construction of P-channel MOSFET: (a) Enhancement, and (b) Depletion

Operation of MOSFET (N-channel)

The operation of MOSFET transistors is same as the JFET. The main difference is, due to the oxide layer between the gate and channel, we can apply both positive and negative voltage to the gate, but current will not flow through the the gate. The output characteristics, and the transfer characteristics of a depletion MOSFET is shown in Fig.4-21. Here, the the transistor works for both positive and negative voltage of V_{GS}, called ***Enhancement Mode*** and, ***Depletion Mode***, respectively.

On the other hand, enhancement MOSFET works only when positive voltage is applied at the Gate termianl.

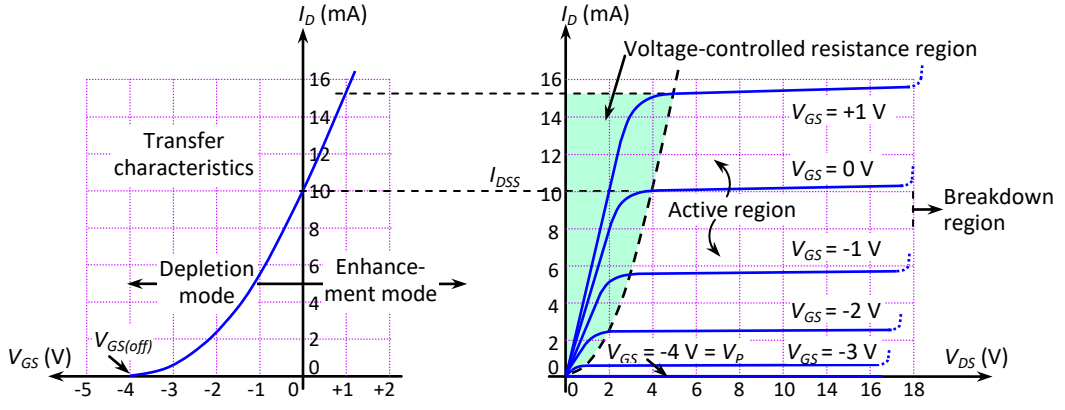


Fig.4-21: Characteristic curves of depletion MOSFET: (a) Transfer characteristics, and (b) Output characteristics.

CHAPTER

5

Feedback in Amplifiers

5.1 Feedback Theory

The general structure of a feedback amplifier may be depicted by the signal flow diagram of Fig.5-1. Here x may be a voltage or current signal.

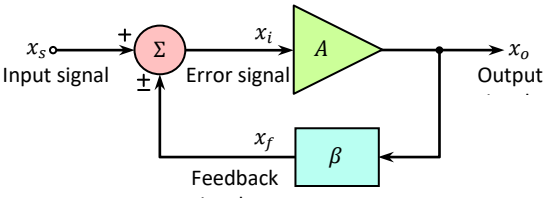


Fig.5-1: General feedback circuit

The amplifier (to which the feedback is applied) has a gain (A) without feedback, called ***open-loop gain***. This amplifier amplifies the input signal, so the output will be $x_o = Ax_i$.

The feedback unit (β) may vary from a simple direct connection to a complex circuit. This block is connected between input and output and produces a feedback path. When feedback is applied to an amplifier, it is called ***closed-loop amplifier***. The feedback unit produces a feedback signal x_f (either voltage, v_f, or current, i_f) which is proportional to output signal x_o such that $x_f = \beta x_o$. The fraction $\beta = x_f/x_o$ is called ***feedback factor***. The feedback signal (x_f) has been applied to a summing unit, that combines the feedback signal, x_f, with the input signal, x_s. Depending on the polarity of x_f, the summing unit may add or subtract x_f from the input signal x_s. Thus the summing unit produces a resultant signal

$x_i = x_s \pm x_f$ which is called the ***error signal***. This error signal (x_i) is applied to the amplifier. So the output of the amplifier will be,

$$x_o = Ax_i = A(x_s \pm x_f)$$

But we know $x_f = \beta x_o$. Putting this value into the above equation we get,

$$x_o = A(x_s \pm \beta x_o)$$

or, $$x_o = Ax_s \pm A\beta x_o$$

or, $$x_o \mp A\beta x_o = Ax_s$$

or, $$x_o(1 \mp A\beta) = Ax_s$$

Therefore, the gain of the amplifier with feedback (denoted by A_f) will be,

$$\boxed{A_f = \frac{x_o}{x_s} = \frac{A}{1 \mp A\beta}} \quad (5\text{-}1)$$

or, $$\boxed{A_f = \frac{A}{1 + A\beta}\ (\text{for negative feedback})} \quad (5\text{-}2)$$

or, $$\boxed{A_f = \frac{A}{1 - A\beta}\ (\text{for positive feedback})} \quad (5\text{-}3)$$

Here, A_f is the gain of the amplifier with feedback. This gain is also called ***closed-loop gain***. The product of amplifier's gain (A) and feedback factor (β) is called ***loop-gain***.

Depending on the polarity (or phase) of x_f there are two types of feedback. If x_f is positive (x_f adds with x_s), it is called ***positive feedback***, and if x_f is negative (x_f is subtracted from x_s) it is called ***negative feedback***. The closed-loop gains of these amplifiers are given by Equ.(5-2) & (5-3).

Example 5-1

An amplifier has a voltage gain of 100. If negative feedback is applied to this amplifier, the overall gain (closed-loop gain) falls to 10. (i) Calculate the feedback factor (β). (ii) If the value of β is maintained, calculate the required gain of the amplifier to make the overall gain 11.

Solution:

(i) In the first case, $A = 100$, and $A_f = 10$.

Using Equ.(5-2) $$A_f = \frac{A}{1 + A\beta}\ or, 10 = \frac{100}{1 + 100\beta}$$

or, $$10 + 1000\beta = 100$$

or, $$\beta = \frac{90}{1000} = 0.09\ [\text{Ans.}]$$

(ii) For the second case, $\beta = 0.09$, and $A_f = 11$.

Using Equ.(5-2) $$A_f = \frac{A}{1 + A\beta} \; or, 11 = \frac{A}{1 + A \times 0.09}$$

$or,$ $$11 + 0.99\,A = A$$

$or,$ $$0.01A = 11$$

$or,$ $$A = \frac{11}{0.01} = 1100 \; [\text{Ans.}]$$

Comments: Here a large negative feedback is used. So open loop gain 100 falls to only 10. For this large negative feedback A_f has been very stable. So for a small change in A_f (1) a large change in A (1000) is required.

5.2 Types of Feedback Amplifiers

Already we have mentioned that depending on the phase (or polarity) of feedback signal, there are two types of feedback. These are: ***Negative Feedback***, and ***Positive Feedback***.

Positive Feedback Amplifier

If the feedback signal (x_f) is mixed with the input signal (x_s) in such a way that the overall input to the amplifier increases, then it is called ***positive feedback***. As the input signal is increased, positive feedback increases the gain of the amplifier as shown in Fig.5-2(a). Positive feedback is

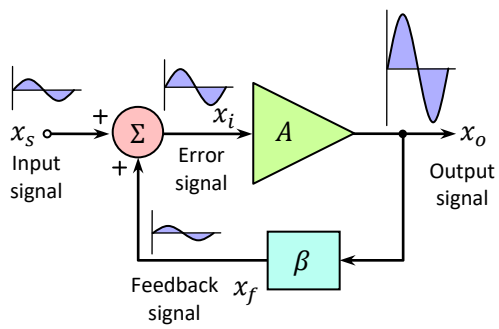


Fig.5-2 (a): Positive feedback

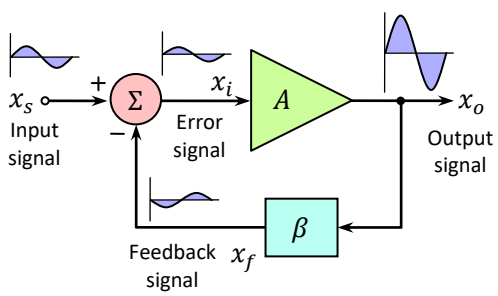


Fig.5-2 (b): Negative feedback

also called ***direct feedback***. As positive feedback has a lot of disadvantages. Generally it is not often used in amplifiers. But, it amplifies power of the original signal and can be used in oscillator circuits. The main disadvantages of positive feedback are given below:

- Lower input impedance
- Unstabilized voltage gain
- Increased output impedance
- Increased noise, and
- Increased nonlinear distortion

Negative Feedback Amplifier

If the feedback signal is mixed with the input signal in such a way that the overall input to the amplifier decreases, then it is called ***negative feedback***. As the input signal is decreased, negative feedback decreases the gain of the amplifier as shown in Fig.5-2(b). Negative feedback is also called ***inverse feedback***. Negative feedback provides many advantages, and hence it is regularly used in amplifiers. The main advantages of negative feedback are given below:

- Better stabilized voltage gain
- Higher input impedance
- Improved frequency response
- Lower output impedance
- Reduced noise
- More linear operation

5.3 Feedback Amplifier Topologies

The feedback signal may be proportional to the output voltage or output current. Similarly the feedback signal itself may be either a voltage signal or a current signal. The combinations of these variations result in four types of topologies of designing feedback amplifiers. These are:

- Voltage Series Feedback Amplifier
- Voltage Shunt Feedback Amplifier
- Current Series Feedback Amplifier
- Current Shunt Feedback Amplifier

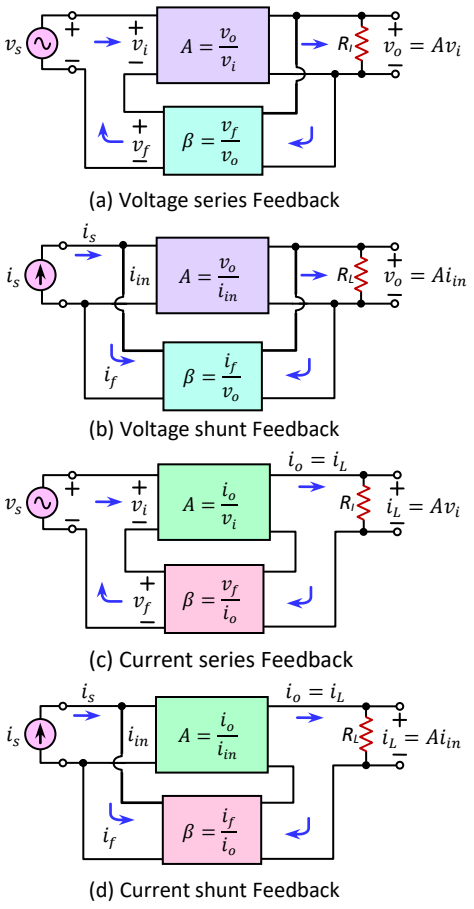


Fig.5-3: Four topologies of feedback amplifier circuits

In these names of topologies, the first term (either voltage or current) indicates what type of parameter (voltage/current) the feedback signal (v_f or i_f) is proportional to. The second term (series or shunt) means how the feedback signal is connected to the source signal. For example, ***voltage series feedback*** means the feedback signal is proportional to output voltage and it is connected in series with source signal [Fig.5-3(a)]. In the same way, ***current shunt feedback*** means the feedback signal is proportional to output current and it is connected in parallel to the source signal [Fig.5-3(d)]. To generate a feedback signal proportional to output voltage, the whole output voltage has to be applied to the input of feedback network, that is, the two input terminals of the feedback network have to be connected in parallel with load resistance, R_L [as shown in Fig.5-3(a, b)].

Similarly, To generate a feedback signal proportional to output current, the whole output current has to be applied to the feedback network, that is, the input side of feedback network has to be connected in series with load resistance, R_L [as shown in Fig.5-3(c, d)].

CHAPTER

6

Operational Amplifiers

6.1 Introduction

In electronics, the most important and common analog ***integrated circuit*** (IC) is the operational amplifier or shortly op-amp. An ***operational amplifier*** is a high-gain amplifier circuit with two high-impedance input terminals and one low-impedance output terminal as shown in Fig.6-1. As operational amplifiers are built in IC, they posses many advantages like: small size, low cost, high reliability, low offset voltage and current, temperature tracking properties etc.

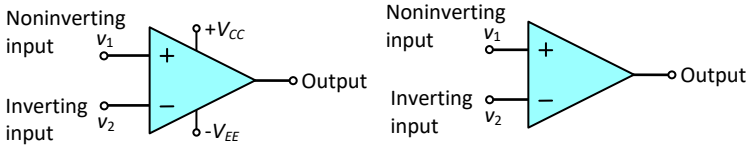


Fig.6-1: Electrical symbol of operational amplifier

6.2 Op-amp Symbol and Equivalent Circuit

The operational amplifier is represented by a symbol as shown in Fig.6-1. The symbol of an op-amp has two inputs: one is inverting input denoted by '-' sign and the other is noninverting input denoted by '+' sign. The symbol has one output. Power supply connection may be shown in the symbol or not. A

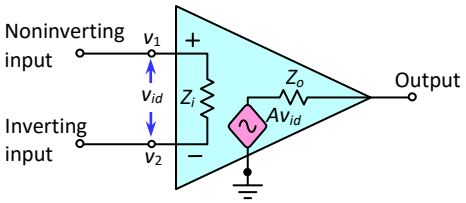


Fig.6-2: Equivalent circuit of operational

signal (AC or DC voltage) applied to noninverting input, produces an in-phase (or same polarity) signal at the output. On the other hand, a signal applied to inverting input, produces an out of phase (or opposite polarity) signal at the output.

The equivalent circuit of an operational amplifier is shown in Fig.6-2. The input circuit is represented by a very large impedance, Z_i and the output circuit is represented by a dependant voltage source ($A_v v_{id}$) and a series output impedance, Z_o. The voltage level of the dependant voltage source is the product of the gain of the op-amp (A) and the difference of two voltages ($v_{id} = v_1 - v_2$) applied to the inputs, that is, Av_{id}.

This IC is mainly manufactured in three forms: 8-pin SOIC package, 8-pin Dual-in-line package, and TO5-8 metal can form as shown in Fig.6-4.

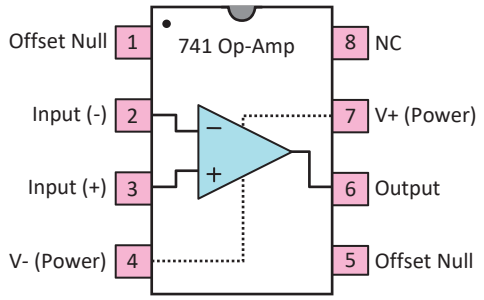


Fig.6-3: Pin diagram of 741 op-amp

(a) (b) (c)

Fig.6-4: Op-amp IC package: (a) 8-pin DIP, (b) 8-pin SOIC, and (c) TO5-8 metal can

6.3 Characteristics of Ideal and Practical Op-Amp

Although we cannot fabricate an ideal op-amp, we can imagine an op-amp with ideal characteristics. Generally the characteristics of practical op-amp are compared with those of an ideal op-amp. The flowing table gives a comparison between the ideal and practical operational amplifiers.

Table 5-1-: Characteristics of an ideal and practical op-amp

Parameters	Ideal Op-amp	Practical Op-amp
Open-loop gain (A)	Infinite	Very high (>10000)
Bandwidth (BW)	Infinite	High (≈ 10 MHz)
CMRR	Infinite	High (> 60 dB)
Input impedance (Z_{in})	Infinite	Very high (>1 MΩ)
Output impedance (Z_o)	Zero	Very low (< 100 Ω)
Input bias currents (I_B)	Zero	Very low (< 50 nA)
Input offset voltage (V_{io})	Zero	Low (< 10 mV)
Input offset current (I_{io})	Zero	Low (< 50 nA)
Slew rate (SR)	Infinite	High (few V/µs)
Drift	Zero	Low

6.4 Applications of Op-Amps

The op-amp has very high voltage gain but very small bandwidth. Therefore, to increase the bandwidth and gain stability, negative feedback is used in op-amp amplifiers. For the comparator and oscillator circuits, positive feedback is used. Some of the op-amp circuits (applications) are described below.

6.5 Noninverting Amplifier

Fig.6-5 shows the circuit diagram of a ***noninverting amplifier***. The feedback network is constructed using the resistors R_1 and R_f. As the input signal (v_i) is applied to the noninverting terminal, this circuit is called ***closed-loop noninverting amplifier*** or simply ***noninverting amplifier***. Here, the feedback signal (v_f) is applied to inverting terminal. As shown in the circuit, the overall input voltage to the op-amp will be $v_{id} = v_i - v_f$ that ensure negative feedback. The feedback factor is the ratio of feedback voltage and output voltage, that is,

$$\beta = \frac{v_f}{v_o}$$

Using voltage divider rule,

$$v_f = v_o \times \frac{R_1}{R_1 + R_f}$$

$or,$

$$\frac{v_f}{v_o} = \frac{R_1}{R_1 + R_f}$$

$\therefore$

$$\boxed{\beta = \frac{R_1}{R_1 + R_f}} \qquad (6\text{-}1)$$

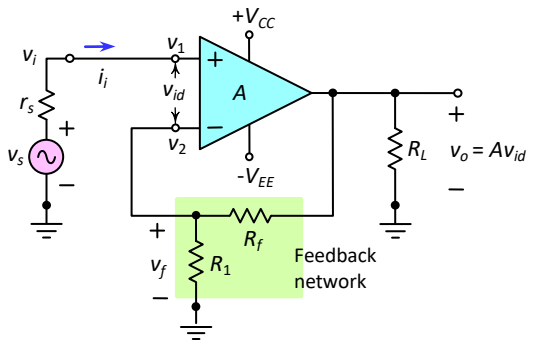


Fig.6-5: Noninverting amplifier

The voltage gain (with feedback) of this amplifier will be inverse of the feedback factor,

$\therefore$

$$\boxed{A_f = \frac{1}{\beta} = 1 + \frac{R_f}{R_1}} \qquad (6\text{-}2)$$

The input impedance, and the output impedance of the circuit will be,

$\therefore$

$$\boxed{Z_{if} = Z_i(1 + A\beta)} \qquad (6\text{-}3)$$

$$\boxed{Z_{of} = \frac{Z_o}{1 + A\beta}} \qquad (6\text{-}4)$$

Here, Z_i, and Z_o are the input impedance and output impedance, respectively of the op-amp without feedback.

The bandwidth of an amplifier is the difference between the higher cutoff frequency and the lower cutoff frequency. As op-amps can amplify DC signal, its lower cutoff frequency is 0. So, the bandwidth of an op-amp will be simply its higher cutoff frequency (f_o). If the bandwidth of the op-amp is f_o the increased bandwidth due to the negative feedback will be,

$\therefore$

$$\boxed{f_f = f_o(1 + \beta A)} \qquad (6\text{-}5)$$

From this equation, we find that the closed-loop bandwidth has been increased by a factor of $(1 + \beta A)$.

Example 6-1

For the noninverting amplifier of Fig.6-5, assume $A = 2 \times 10^5$, $f_o = 5$ Hz, $Z_i = 1$ MΩ, $Z_o = 75$ Ω, $R_f = 510$ k, and $R_1 = 10$ k. Determine closed-loop gain, closed-loop input impedance, closed-loop output impedance, and bandwidth.

Solution:

Using Equ.(6-1), $$\beta = \frac{R_1}{R_1 + R_F} = \frac{10\text{ k}}{10\text{ k} + 510\text{ k}} \approx 0.0192$$

Closed-loop gain:

Using Equ.(6-2), $$A_f = 1 + \frac{R_F}{R_1} = 1 + \frac{510\text{ k}}{10\text{ k}} = 52\ [\text{Ans.}]$$

Closed-loop input impedance:

Using Equ.(6-3), $$Z_{if} = Z_i(1 + A\beta) = 1\text{ M}\Omega(1 + 2 \times 10^5 \times 0.0192)$$

$\therefore$ $$Z_{if} \approx 3.84\text{ G}\Omega\ [\text{Ans.}]$$

Closed-loop output impedance:

Using Equ.(6-4), $$Z_{of} = \frac{Z_o}{(1 + A\beta)} = \frac{75}{(1 + 2 \times 10^5 \times 0.0192)}$$

$\therefore$ $$Z_{of} \approx 0.02\ \Omega\ [\text{Ans.}]$$

Closed-loop bandwidth:

Using Equ.(6-5), $$f_f = f_o(1 + \beta A) = 5\text{ Hz}(1 + 2 \times 10^5 \times 0.0192)$$

$\therefore$ $$f_f \approx 19.2\text{ kHz}\ [\text{Ans.}]$$

Comments: Due to the negative feedback, the gain has been decreased, but other parameters have been improved.

Inverting Amplifier

Fig.6-6 shows the circuit diagram of a closed-loop inverting amplifier. In this circuit, the feedback network is constructed using the resistors R_1 and R_f. As the input signal is applied to the inverting terminal and feedback is used, this circuit is called ***closed-loop inverting amplifier*** or simply ***inverting amplifier***. Here, the full output voltage is applied to the feedback network, and the feedback current (i_f) is connected in parallel with the input signal. Here, the type of the feedback is negative feedback. The input signal will be amplified by the op-amp and the output will be 180° out of phase with respect to the input.

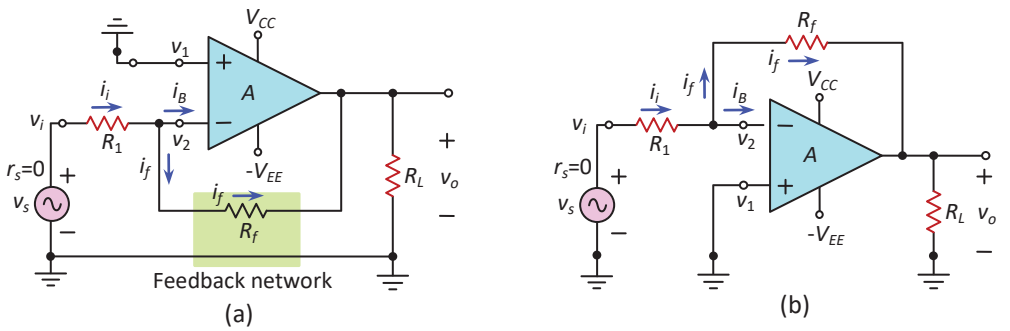


Fig.6-6: Closed-loop inverting amplifier: (a) Circuit with feedback concept, (b) Circuit with amplifier concept

Although this circuit uses voltage shunt feedback, the feedback factor is calculated as $\beta = v_f/v_o = R_1/(R_f + R_1)$.

The voltage gain, input impedance, and output impedance expressions are given below,

$$\boxed{A_f = -\frac{R_f}{R_1}} \tag{6-6}$$

$$\boxed{Z_{if} = R_1} \tag{6-7}$$

$$\boxed{Z_{of} = \frac{Z_o}{1 + A\beta}} \tag{6-8}$$

Example 6-2

For the inverting amplifier of Fig.6-6, assume $A = 2 \times 10^5$, UGB $= 1$ MHz, $Z_i = 1$ MΩ, $Z_o = 75\ \Omega$, $R_f = 470\ k$, and $R_1 = 10$ k. Determine closed-loop gain, closed-loop input impedance, and closed-loop output impedance.

Solution:

Closed-loop gain:

Using Equ.(6-6), $$A_f = -\frac{R_f}{R_1} = -\frac{470\text{ k}}{10\text{ k}} = -47\ [\text{Ans.}]$$

Closed-loop input impedance:

Using Equ.(6-7), $$Z_{if} = R_1 = 10\text{ k}\ [\text{Ans.}]$$

The value of feedback factor will be $\beta = R_1/(R_f + R_1) = 10\text{ k}/(470\text{ k} + 10\text{ k}) = 0.021$.

Closed-loop output impedance:

Using Equ.(6-8), $$Z_{of} = \frac{Z_o}{(1 + A\beta)} = \frac{75}{(1 + 2 \times 10^5 \times 0.021)}$$

$\therefore$ $$Z_{of} \approx 0.018\ \Omega\ [\text{Ans.}]$$

Comments: Inverting amplifier gives less gain, lower input impedance and lower output impedance.

6.6 Virtual Ground in Inverting Amplifier

As shown in Fig.6-7, the noninverting terminal is directly connected to ground, and the signal is applied to the inverting terminal via resistor R_1. As long as the circuit works linearly, the potential at the inverting terminal is ***zero***. We also know that the potential of ***ground terminal*** is also zero. For this reason, the inverting terminal can be considered as ***ground***. However, a ***true ground*** can source or sink infinite amount of current. But, the inverting terminal cannot source or sink large current, due to the high input impedance of op-amp. For this reason the inverting terminal of the closed-loop inverting amplifier is called ***virtual ground***. For the op-amp, we can write

$$v_o = Av_{id} = A(v_1 - v_2)$$

$$\therefore \quad v_1 - v_2 = \frac{v_o}{A}$$

As, the open-loop gain of an op-amp (A) is very large (ideally infinity), we can write,

$$v_1 - v_2 = \frac{v_o}{A} \approx \frac{v_o}{\infty} = 0$$

$$\therefore \quad v_2 = v_1$$

But, $v_1 = 0$, because the noninverting terminal is directly connected to ground. Therefore,

$$v_2 = v_1 = 0$$

In this circuit the noninverting terminal is ***true ground*** and the inverting terminal is ***virtually ground***. If the negative feedback is removed from this circuit, it will not work linearly and then, the inverting terminal will no longer be virtual ground.

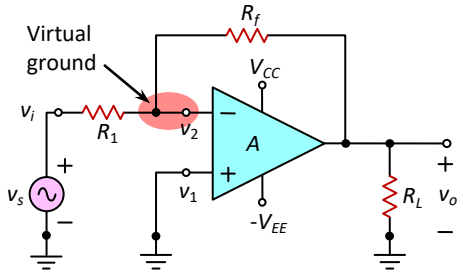


Fig.6-7: Virtual ground in inverting amplifier

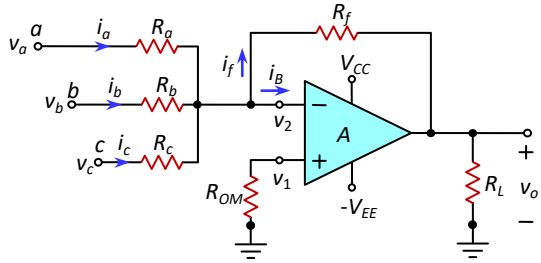


Fig.6-8: Inverting summing amplifier

Summing Amplifier

We can use Op-Amp as a summing amplifier as shown in Fig.6-8. The output of this amplifier will be the sum of input voltages and can be calculated as,

$$\boxed{v_o = -\left(\frac{R_f}{R_a}v_a + \frac{R_f}{R_b}v_b + \frac{R_f}{R_c}v_c\right)}$$

CHAPTER 7

Power Amplifiers

7.1 Introduction

In general, a practical amplifying system consists of several stages that amplify weak signal (received at the input stage) until sufficient power is available to drive the output devices. In audio amplifier system, the output device is mainly a loudspeaker while in a control system it may be a motor or some other output loads. As shown in Fig.7-1, the first stage of an amplifier system is a voltage amplifier that amplifies the voltage levels of very weak signals.

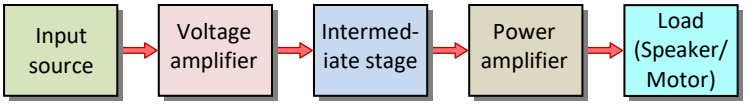


Fig.7-1: Block diagram of an amplifier system

As the name implies, a ***power amplifier*** is one that amplifies the power (or current) levels of signals and delivers that large amount of power to a load. Generally, power amplifiers increase only the current level of the signals which are already amplified by voltage amplifiers. So the signals operated by power amplifiers have large voltage swings (large amplitudes) and the device operates over the entire range of its output characteristics (load line). For this reason, power amplifiers are also called ***large signal amplifiers***.

7.2 Classification of Power Amplifiers

The main operating characteristics of an amplifier are linearity, signal gain, efficiency and power output. Generally, power

amplifiers are used to drive a loudspeaker load. A typical loudspeaker has an impedance of 4 Ω to 16 Ω, thus a power amplifier must be able to supply the high peak current required to drive the low impedance loads.

One method used to distinguish the electrical characteristics of different types of amplifiers is by ***class***.

The most commonly constructed amplifier classes which are mainly used as audio amplifiers are: class-A (360° conduction), B (90° conduction), AB (more than 90° but less than 360° conduction) and C (less than 90° conduction) amplifiers. As shown in Fig.7-2, the efficiency of power amplifiers increases from class-A to class-C.

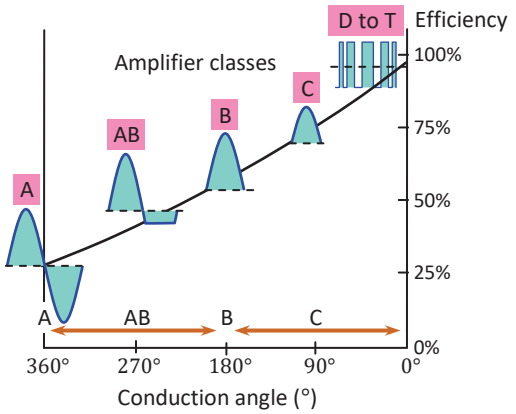


Fig.7-2: Waveforms (conduction angles) of different amplifier classes

7.3 Push-Pull Amplifier with Output Transformer

A push-pull power amplifier is shown in Fig.7-3. It consists of a transformer and two NPN power transistors. The primary winding of the transformer is connected to the transistor collectors, and its center tap is connected to supply voltage, $+V_{CC}$. The center tap is an electrical connection made at the center of the winding, so there are equal number of turns between each end of the winding and the center tap. To drive this amplifier a preamplifier is necessary that produces two out-of-phase signals (v_{i1}, and v_{i2}) on the bases of Q_1 and Q_2. Notice that the transistor bases are grounded via resistors R_{B1} and R_{B2} and hence both transistors are biased at cut-off. So, this is a class-B amplifier.

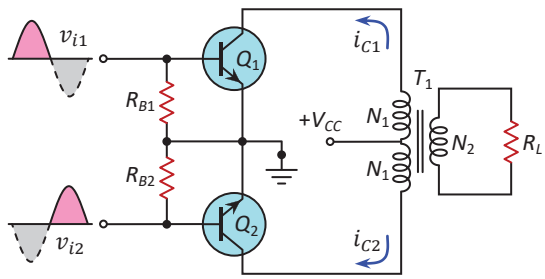
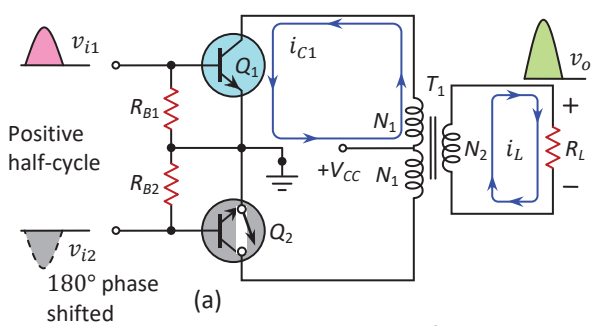


Fig.7-3: Push-pull amplifier with transformer



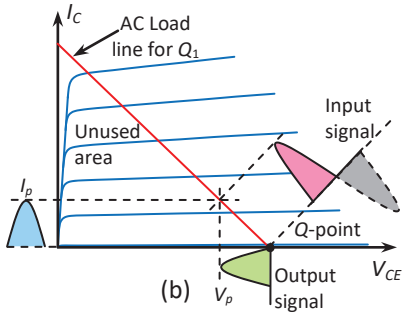


Fig.7-4: Operation of push-pull amplifier for positive half-cycle

Fig.7-4, and Fig.7-5 illustrate how current flows through the amplifier during a positive half-cycle and a negative half-cycle of input. In Fig.7-4(a), the input to Q_1 is positive half-cycle, and since the input to Q_2 is out-of-phase, Q_2 is driven by a negative half-cycle. Consequently, the positive base voltage on Q_1 turns it ON and conducts current in counterclockwise direction as shown in the figure. The negative base voltage on Q_2 keeps this transistor cut-off (open circuit). Current flowing in the upper half of the transformer's primary induces current in the secondary winding, and current flows through the load.

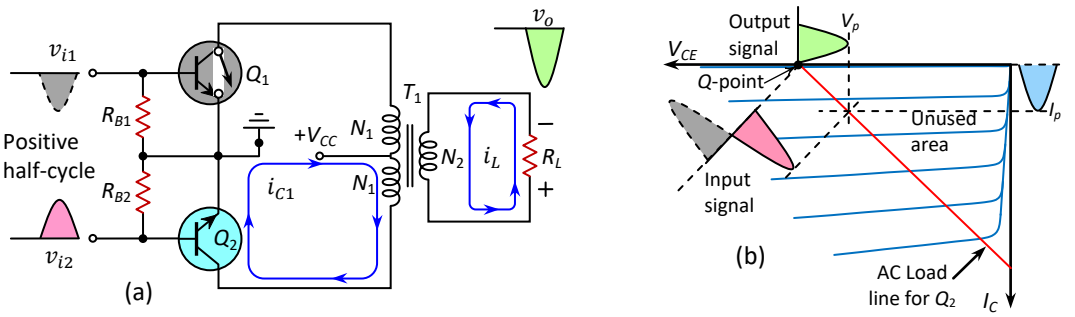


Fig.7-5: Operation of push-pull amplifier for negative half-cycle

Fig.7-5 shows the situation when the input signal on the base of Q_1 is negative, and on the base of Q_2 is positive. Therefore, Q_2 conducts current in clockwise direction but Q_1 is cut-off. Current induced in the secondary winding is in opposite direction than that shown in Fig.7-4(a). The overall result is that current flows through the load in one direction for positive input signal, and in opposite direction for negative input signal. The output characteristics of the transistors with the load line and operating points are shown in Fig.7-4(b) and Fig.7-5(b). The combine response of these two transistors can be shown as in Fig.7-6. Note that the characteristics of transistor Q_2 have been drawn upside down, to draw a continuous load line. In response to the input signal, the Q-point will swing over the entire load line from point A to B. The swing of Q-point will produce swings in output voltage and output current.

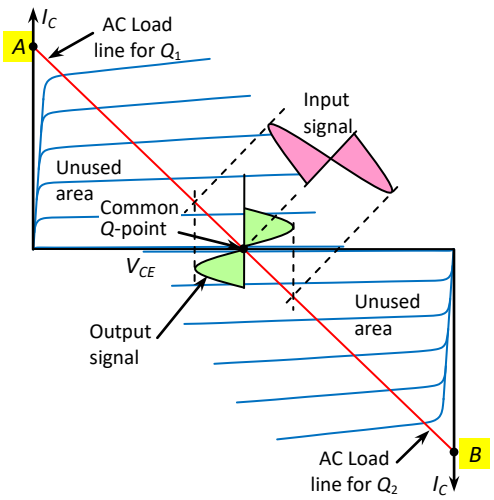


Fig.7-6: Combined AC load line of a class-B amplifier drawn on the composite BJT characteristics

7.3.1 Cross-Over Distortion

Although class-B amplifier provides high efficiency, they suffer from cross-over distortion. ***Cross-over distortion*** is a type of distortion caused by switching of current from one transistor to another. The term cross-over signifies the ***crossing over*** of the signal between transistors Q_1 and Q_2 and vice versa. In the amplifier circuit of Fig.7-3, both the transistors are biased at the cut-off point (zero base voltage at no signal condition) and therefore transistors are not conducting for

DC condition. Consider a positive-going swing. As long as the input is less than the required forward V_{BE} drop (≈ 0.65 V) of transistor Q_1, it will remain off or conduct very little current-same as a diode operation. In fact, due to the nonlinear behavior of the input characteristics of the transistor, the base current does not increase in proportion to the input signal. This nonlinearity is prominent at the low voltage region (0 to 0.5 V). At this region, the input current becomes distorted (shape change). Being an amplified version of base current, the output current (hence output voltage) also becomes distorted as shown in Fig.7-7. The same thing happens for the transistor Q_2, for the negative half-cycles of input.

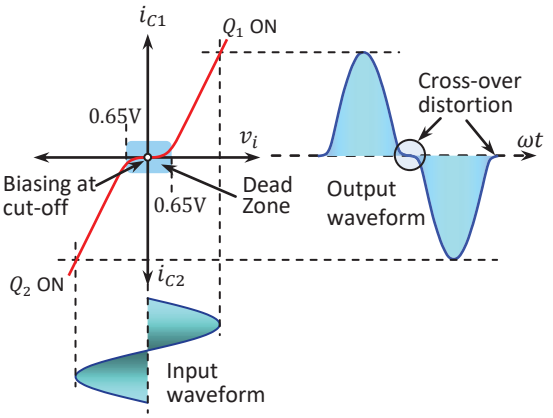


Fig.7-7: Cross-over distortion in Class-B amplifier

7.4 Class-AB Amplifier

Cross-over distortion in a push-pull amplifier can be eliminated by biasing each transistor slightly into conduction, that is, setting the operating points just slightly above the cut-off point. Therefore, the transistors conduct current for a little more than 180° (one half-cycle = 180°). A small forward biasing voltage is applied across each base-emitter junction that causes a small base current even in no-signal conditions (DC condition). Now, it is not necessary for the input signal to overcome the junction barrier voltage and to start conduction of the transistors. Thus, the cross-over distortion is eliminated. The amplifiers with the transistors biased in such a way, is called a ***class-AB amplifier***. Fig.7-8 shows a class-AB amplifier.

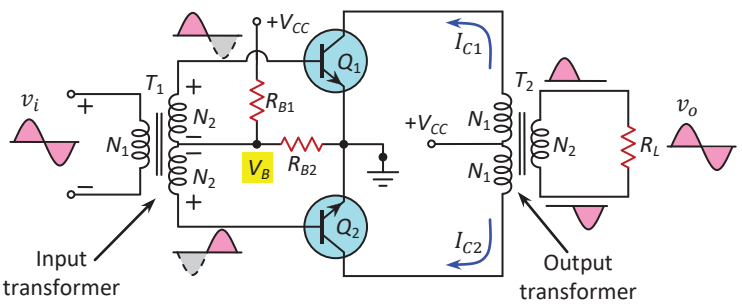


Fig.7-8: Class-AB push-pull amplifier with input and output transformers

In this circuit, a simple voltage-divider biasing network, consisting of R_{B1} and R_{B2}, is used to produce the biasing voltage, V_B, which is applied to the bases of Q_1, and Q_2 via the secondary coil of the transformer. As the DC resistance of the transformer windings is very small, the biasing voltage will be applied to the bases of the transistors, without any significant drop.

When a transistor is biased slightly into conduction, output current will flow during more than one-half cycle of a sine-wave input, as illustrated in Fig.7-9. While class-AB operation reduces

cross-over distortion in a push-pull amplifier, it has the disadvantage of reducing amplifier efficiency.

7.5 The TDA203

The TDA2030 is a monolithic integrated circuit in Pentawatt package (zigzag package), intended for use as a low to medium frequency class-AB amplifier. Typically it provides 14 W output power (with 0.5% distortion) to a 4 Ω load with ± 14 V or 28 V supply voltage. The guaranteed output power is 12 W on a 4 Ω load and 8 W on an 8 Ω load. The TDA2030 provides high output current and has very low harmonic and cross-over distortion. Further, the device incorporates an original short-circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included. The TDA2030 is a 5-pin IC and available in TO220 package. A photograph and the pin-diagram of this IC are shown in Fig.7-10.

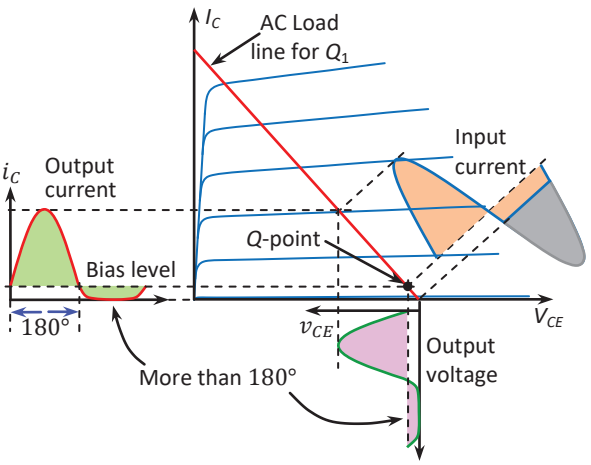


Fig.7-9: Class-AB operation: output current flows more than 180°, but less than 360° of input signal

A 14 W Amplifier Circuit Using TDA2030

The TDA2030 IC subwoofer (mid-range frequency) circuit using 28 V single power supply is shown in Fig.7-11. The input signal is applied to a 22 k potentiometer to control the volume of the amplifier. From this potentiometer the input signal is applied to the noninverting terminal (pin1) through a 2.2 µF capacitor (C_1). This input capacitor and the input resistor $R_1 = 100$ k set the lower cut-off frequency of the amplifier. The R_4 resistor, which is connected between pins 2 & 4, is known as feedback resistor. This resistor and R_3 determine the AC closed-loop gain of the amplifier. Capacitor C_4 is short for AC signal and open for DC signal. Thus, for DC signal the amplifier will work as buffer which reduces offset voltage at the output.

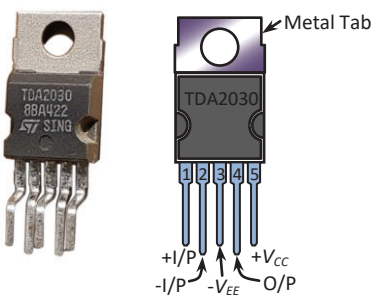


Fig.7-10: Photograph and pin diagram of TDA2030 IC

The output of the IC is connected to the loudspeaker through the 2000 µF series capacitor (C_7) which isolates the DC voltage from the load. This circuit uses 4 Ω to 6 Ω-ohm speakers to generate 12 W output. The heat (high temperature) developed in this IC should be removed by using a heat sink. The combination of the output resistor R_5 and capacitor C_5 are used to balance the load impedance. They help in avoiding the surplus noises within the speaker. The diodes (1N4001) connected from the output terminal (pin 4) to the supply rails protect the internal

power transistors from any high voltage generated by inductive load. Capacitors C_3 and C_6 are power supply decoupling capacitors that provides surge current to the load.

Although the device incorporates a short circuit protection system and a conventional thermal shut-down system, a heat sink must be used for the TDA2030 IC. If the junction temperature increases up to 150°C, the thermal shut-down mechanism simply reduces the power dissipation and the current consumption of the IC.

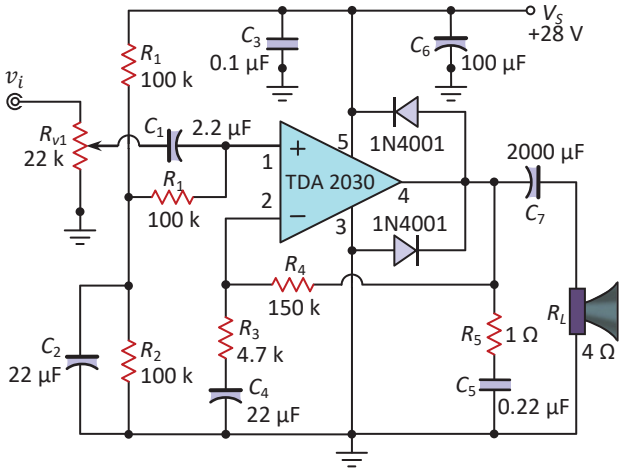


Fig.7-11: A 14 W power amplifier using TDA2030 IC

A 35 W Bridge Amplifier Using TDA2030

Typically TDA2030 provides 14 W output power at ± 14 V or 28 V as shown in Fig.7-11. However, with a split supply voltage of ±15 V it is possible to design 35 W amplifier using the TDA2030 in a bridge connection as shown in Fig.7-12. This type of amplifier is also called ***Bridge Tied Load*** (BTL) amplifier.

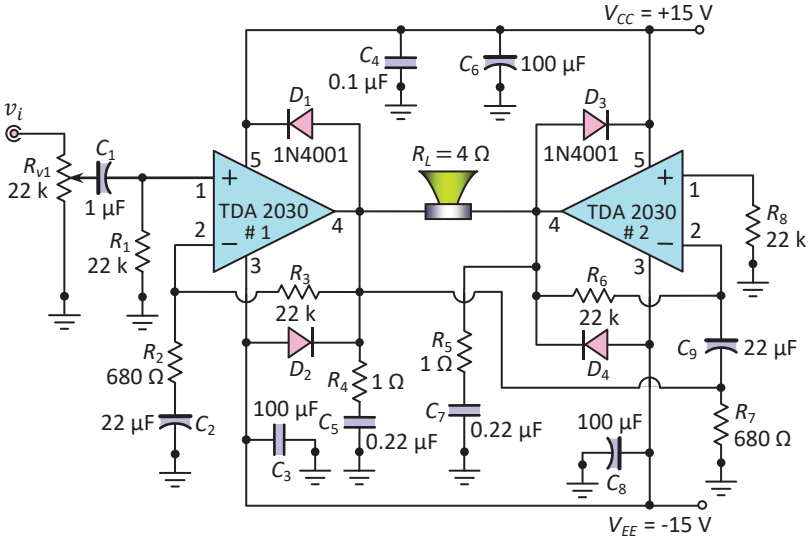


Fig.7-12: A 35 W bridge power amplifier using TDA2030 IC

In this circuit there are two TDA2030 ICs that are connected together. The components connection to each IC is almost similar to that of Fig.7-11. Only the IC # 2 is connected in slightly different way. As shown in the Fig.7-12, the noninverting terminal of this IC is grounded through a 22 k resistor and the output from TDA2030 #1 is connected to the inverting input of TDA2030 #2 via C_9. Thus, the output of this IC (IC #2) will be 180° outoff phase from that of IC #1. Therefore, both the output voltages will be added across the load (loud speaker) and a highly amplified signal will be developed.

CHAPTER
8

Oscillators

8.1 Introduction

An ***oscillator*** is a circuit that generates an AC output signal without any input signal or an ***oscillator*** is a circuit that converts DC energy into AC energy at very high frequency. Generally an oscillator is made by using an ***amplifier*** and a ***positive feedback network***. Although amplifiers use negative feedback to provide stability, oscillators use positive feedback to generate undamped continuous oscillations. When there is no input signal to an amplifier, there is no output signal. On the other hand, an oscillator does not require any external signal as input. Without any input signal it can produce output signal so long as the DC power supply is connected. The output of the oscillators may be sinusoidal or non-sinusoidal. Among the non-sinusoidal the most common waveforms are: ***square wave***, ***triangular wave***, ***saw-tooth wave***, etc.

8.2 Classifications of Oscillators

Oscillators are classified into several types based on various factors: like the shape of waveform, range of frequency, etc. The followings are the broad classification of oscillators.

According to the Generated Waveform

Based on the output waveforms, oscillators are classified as,

Sinusoidal Oscillators: This type of oscillator generates sinusoidal outputs. They are most commonly used in electronics. Examples of some sinusoidal oscillators are

- Tuned-circuits or *LC* feedback oscillators such as Hartley, Colpitts and Clapp oscillator etc.
- *RC* phase-shift, Wien-bridge oscillators etc.
- Negative-resistance oscillators such as tunnel diode oscillator.
- Crystal oscillators such as Pierce oscillator.
- Heterodyne or beat-frequency oscillator (BFO).

Non-sinusoidal Oscillators: This type of oscillators generates non-sinusoidal output. Among various non-sinusoidal oscillators, the most common waveforms are triangular wave, square wave, rectangular wave, saw tooth wave etc.

8.3 Oscillator Theory

The main statement of the oscillator is that the oscillation is achieved through positive feedback which generates the output signal without input signal.

Let us consider a non-inverting amplifier with a voltage gain A_v and a positive feedback network with feedback factor of β as shown in Fig.8-1.

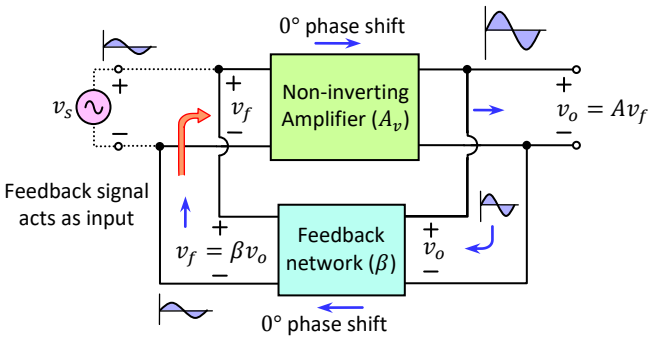


Fig.8-1: Amplifier with positive feedback

Since the amplifier is non-inverting, the output signal v_o is in phase with input v_s. A feedback network feeds a part of v_o to the input and the amount fed back (v_f) depends on the feedback network gain (also called ***feedback factor***) $\boldsymbol{\beta}$ ($= v_f/v_o$). Here, the amplifier produces 0° phase shift, and the feedback network also produces 0° phase shift. Therefore, the total phase shift around the loop is 0° that ensures positive feedback.

The gain of an amplifier with positive feedback is,

$$A_f = \frac{A_v}{1 - A_v\beta} \tag{8-1}$$

Where, $A_v\beta$ (called ***loop-gain***) is the product of ***open-loop gain*** (A_v) and the ***feedback factor*** (β). If the value of loop-gain is unity, that is, if $A_v\beta = 1$, from Equ.(8-1) we find that the gain of the amplifier with feedback will be infinity, that is $A_f = A_v/(1-1) = \infty$. So, if the signal source is disconnected ($v_s = 0$), the amplifier will produce a finite output.

When an oscillator is powered ON some sort of noise, like transient noise, is produced. Though noise has a wide frequency range, only a particular frequency, for which the oscillator is designed, will fulfill the condition of oscillation (described in Section 8-4). At first the gain of the amplifier will a little larger than $1/\beta$ (or $A_v\beta > 1$). So, that particular frequency will gradually be amplified as shown in Fig.8-2. Due to the saturation of the amplifier (and some other energy loss) the output will be fixed to a certain value, and the gain of the amplifier will be adjusted to $A_v = 1/\beta$. Sometimes ***automatic gain control*** (AGC) circuit is used to limit the amplitude of the oscillators.

8.4 Barkhausen Criteria

We have already discussed that an amplifier can work as an oscillator if we add positive feedback to it. An amplifier will work as an oscillator under some conditions. These conditions are called ***Barkhausen criteria***. In fact, Barkhausen criteria are nothing but formal representation of the theory of oscillator.

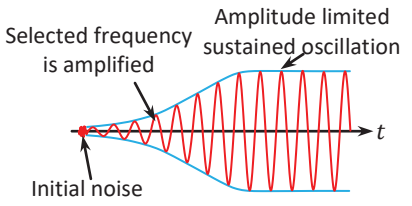


Fig.8-2: Development of output signal in an oscillator

The Barkhausen criteria state the following:

1. The value of the loop-gain ($|A_v\beta|$) of the amplifier must be 1. In fact, at first (during the buildup of output signal) $A_v\beta$ should be slightly greater than 1 and when the output signal is established, $A_v\beta$ should be unity.
2. The phase shift around the loop should be zero or an integer multiple of $360°$, that is $\angle A_v\beta = n \times 360°$, where $n = 0, 1, 2$ etc.

8.5 *RC* Phase Shift Oscillator

The *RC* phase shift oscillator is used to generate a wide range of frequencies, from few Hz to 200 kHz. Fig.8-3 shows the circuit diagram of an RC phase shift oscillator. The common emitter amplifier is biased using a voltage divider network (R_{B1}, R_{B2}). R_E is used to stabilize the DC operating point and R_C is the load resistance of the amplifier. C_{oc} is the output coupling capacitor and C_E is the emitter bypass capacitor. This CE amplifier provides necessary gain and $180°$ phase shift. The frequency selecting network is made using three *RC* circuits that produces another 180° phase shift. Each *RC* network produces $60°$ phase shift as shown in Fig.8-4(a).

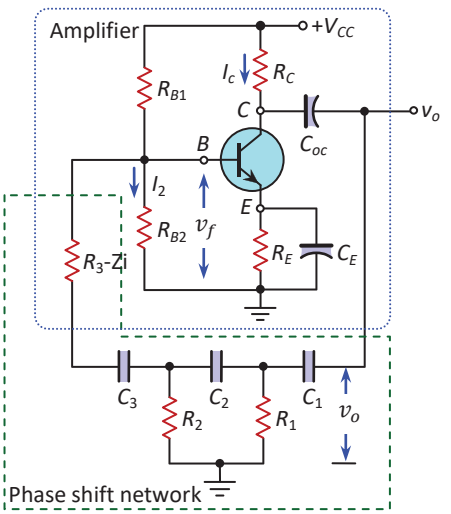
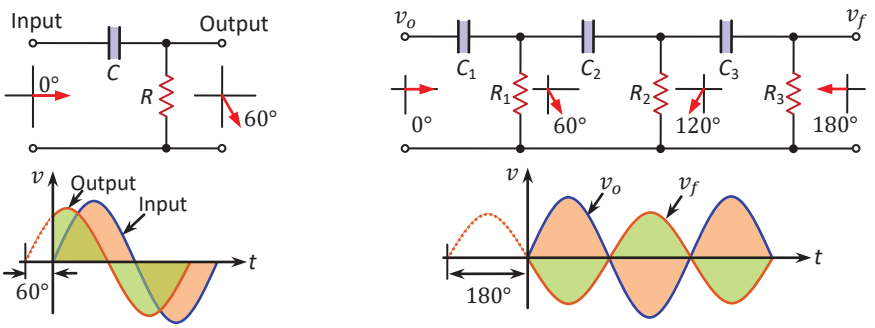


Fig.8-3: *RC* phase shift oscillator

With a proper choice of R and C, total $180°$ phase shift is achieved for the desired frequency.



(a) Single stage *RC* network (b) Three-stage *RC* network

Fig.8-4: Phase shift mechanism in *RC* networks

Circuit Operation:

At first the gain of the amplifier (A_v) will be greater than $1/\beta$, that is $A_v\beta > 1$. When the power is applied to the circuit, electrical noise in the circuit or the turn-ON transients provide an initial signal to start oscillation. The noise has many frequencies. But only a particular frequency, for which the oscillator has been designed, will be $180°$ phase shifted by the RC networks and will be applied to amplifier's input and will be amplified by the amplifier. Now RC network will get an amplified signal, so it will feed a larger signal at the input. Due to this larger input signal, the amplifier will produce more amplified signal at the output. As $A_v > 1/\beta$, a positive regenerative process will continue. When the generated signal attains a substantial amplitude, due to the little nonlinearity of the BJT, A_v will decrease. Thus, a signal of desired frequency with constant amplitude is produced in the circuit. The frequency of oscillation of this oscillator is given by,

$$\boxed{f_o = \frac{1}{2\pi RC\sqrt{6}}} \qquad (8\text{-}2)$$

To satisfy the condition $A_v\beta \geq 1$, the voltage gain of the amplifier should be,

$$\therefore \quad \boxed{|A_v| \geq 29} \qquad (8\text{-}3)$$

Example 8-1

Assume $C_1 = C_2 = C_3 = 420$ pF, $R_1 = R_2 = R_3 - R_{B1}\|R_{B2}\|Z_i = 3.9$ kΩ, and $R_C = 3$ kΩ for the phase shift oscillator of Fig.8-3. Calculate the frequency of oscillation and the gain of the amplifier.

Solution:

Here, $R_3 - R_{B1}\|R_{B2}\|Z_i = 3.9\ \text{k}\Omega$ means that the effective resistance of the third stage is 3.9 kΩ.

Using Equ.(8-2), $$f_o = \frac{1}{2\pi RC\sqrt{6}} = \frac{1}{2\pi \times 3.9\ \text{k} \times 420\ \text{pF} \times \sqrt{6}} = 26\ \text{kHz}\ [\text{Ans.}]$$

Using Equ.(8-3), $$A_v = 29\ [\text{Ans.}]$$

8.6 Phase Shift Oscillator Using Operational Amplifier

Phase shift oscillator can be made using operational amplifier. Fig.8-5 shows a phase shift oscillator using inverting operational amplifier. The inverting amplifier produces amplification and $180°$ phase shift and another $180°$ phase shift is produced by 3-*RC* stages as described for BJT phase shift oscillator. R_3 is the input impedance of the amplifier as well as the resistance of the third RC stage. For simplicity of analysis, we will assume $R_1 = R_2 = R_3 = R$, and $C_1 = C_2 = C_3 = C$. Then, the frequency of oscillation can be calculated using Equ.(8-2),

$$\boxed{f_o = \frac{1}{2\pi RC\sqrt{6}}}$$

By rearranging the above equation, we get $X_C = \sqrt{6}R$. This is a condition to achieve 180° phase reversal in the phase shift network.

The value of feedback factor will be,

$$\boxed{\beta = -\frac{1}{29}} \qquad (8\text{-}4)$$

Therefore, the gain of the inverting amplifier should be,

$$A_v = -\frac{R_f}{R_3} \geq \frac{1}{\beta} = -29$$

$$\therefore \qquad \boxed{R_f \geq 29R_3} \qquad (8\text{-}5)$$

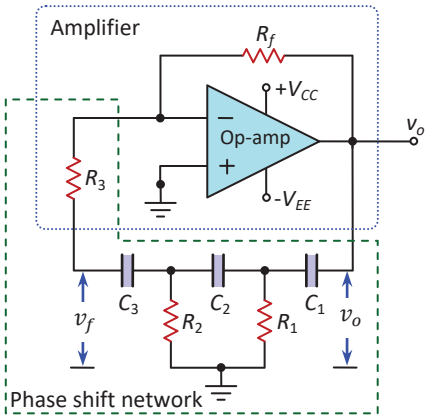


Fig.8-5: *RC* phase shift oscillator using op-amp

Example 15-2

Design a phase shift oscillator using operational amplifier to generate a 5 kHz signal. Assume the supply voltage is ± 12 V.

Solution:

Let us consider $C = 10$ nF. Therefore, using Equ.(8-2),

$$R = \frac{1}{2\pi f_o C\sqrt{6}} = \frac{1}{2\pi \times 5\text{ kHz} \times 1\text{ nF}\sqrt{6}} = 13\text{ k [Ans.]}$$

$$\therefore \qquad R_f \geq 29R_3 \geq 29R \geq 29 \times 13\text{ k} \geq 377\text{ k, use standard } 390\text{ k [Ans.]}$$

Comments: Values of all the resistors will be same, that is, $R_1 = R_2 = R_3 = R = 13\text{ k}\Omega$, but $R_f = 390$ k.

8.7 Colpitts and Hartley Oscillator

Colpitts and Hartley oscillators are LC oscillators that generate medium to high frequencies. The frequency range is 20 KHz to 300 MHz. Fig.8-6 shows the circuit diagram of a Colpitts oscillator. This circuit consists of a CE amplifier with voltage divider bias. The frequency selecting network is made of an inductor L and capacitors C_1 and C_2. This parallel combination of capacitors and inductor is called a ***tank circuit***. The amplifier amplifies the signal and produces 180° phase shift and the frequency selecting network produces another 180° phase shift. C_{ic}, and C_{oc} are the coupling capacitors and C_E is the emitter bypass capacitor. For the frequency of oscillation these capacitors will be short. The coil used in collector is called ***RFC*** (***Radio Frequency Choke***). It provides the necessary DC load resistance (internal resistance) for collector and also prevents AC signal from being short through the voltage source (V_{CC}). As the DC resistance of RFC is small, it provides a wide range to set the operating point and reduces DC power loss.

Circuit Operation:

To understand the operation of an LC oscillator, first we will discuss the operation of an LC tank circuit. An LC tank circuit is a parallel combination of L and C. If a supply voltage is connected momentarily to this tank circuit, the capacitor will immediate be fully charged. If the power supply is disconnected from the tank circuit, a damped oscillation will be produced. The mechanism is illustrated in Fig.8-7. The stored energy in the capacitor will oscillate from capacitor to inductor and vice versa. If there were no loss of energy, this energy conversion process would have been continued infinitely and a pure sinusoidal oscillation was produced. But, due to the resistive loss, mainly in the internal resistance of the inductor, the amplitude of the oscillation gradually decreases, and a damped sinusoidal waveform (voltage and current) is produced.

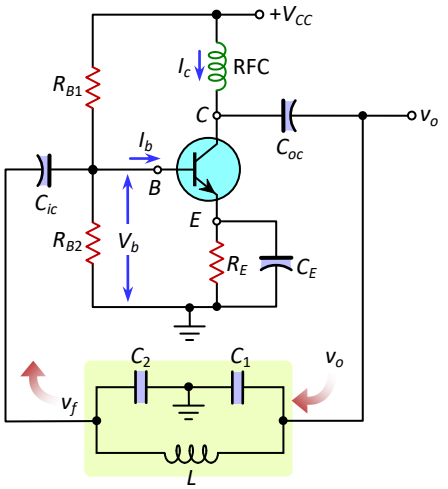


Fig.8-6: Colpitts oscillator

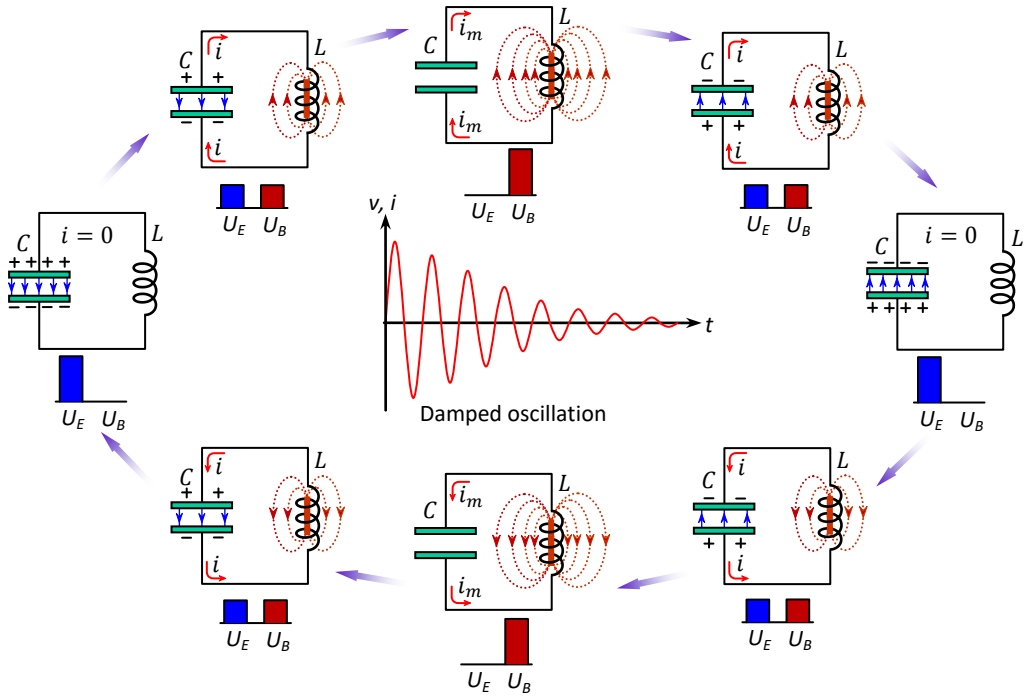


Fig.8-7: Oscillation mechanism of an LC tank circuit

When the supply voltage of the Colpitts oscillator is switched ON, collector current stars to flow and capacitors C_1, and C_2 are charged up. These capacitors and the inductor L work as a tank

circuit and a damped oscillation is produced. But the amplifier compensates the losses and an undamped oscillation is found.

The amount of feedback depends on the ratio of C_2 and C_1 (that is C_1/C_2). Total phase shift around the loop is $360°$. The feedback circuit produces $180°$ phase shift and the amplifier produces another $180°$ phase shift.

The frequency of oscillation will be the resonant frequency of the parallel LC circuit and is given by,

or,
$$\boxed{f_o = \frac{1}{2\pi\sqrt{C_T L}}} \tag{8-6}$$

where, $C_T = C_1 \| C_2 = C_1 C_2/(C_1 + C_2)$.

The minimum value of h_{fe} for the sustained oscillations is given by,

$$h_{fe} = \frac{C_1}{C_2} = \frac{\text{Capcitance connected to collector}}{\text{Capcitance connected to base}} \tag{8-7}$$

8.8 Hartley Oscillator

Hartley oscillator is another common LC oscillator. As shown in Fig.8-8, Hartley oscillator is same as Colpitts oscillator. The only difference is two inductors and one capacitor have been used in the frequency selecting network (tank circuit). The operation process is same as that of Colpitts oscillator. The amount of feedback depends on the values of L_1 and L_2 (that is L_2/L_1). If L_2 increases, its impedance will also increase, hence feedback voltage will increase and vise versa.

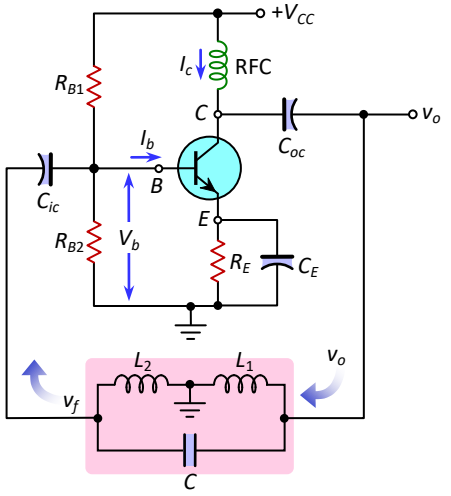


Fig.8-8: Hartley oscillator using BJT

Here also the feedback network will produce $180°$ phase shift, and the CE amplifier will produce another $180°$ phase shift. Thus total phase shift around the loop will be $360°$, which is a requirement for oscillation. The frequency of oscillation will be,

$$\boxed{f_o = \frac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)C}}} \tag{8-8}$$

Here, M is the mutual inductance.

The minimum value of h_{fe} to get the continuous oscillations from the oscillator is

$$h_{fe} = \frac{L_2 + M}{L_1 + M} = \frac{\text{Inductane connected to base}}{\text{Inductane connected to collector}} \tag{8-9}$$

8.9 The Crystal

Some crystals like- quartz, Rochelle salt, tourmaline, corundum etc. show ***piezoelectric effect***. When mechanical stress is applied to a piece of crystal, electric charges are accumulated on the faces of this crystal. This phenomenon is called ***piezoelectric effect***. As shown in Fig.8-9, due to the applied stress the crystal structure is deformed, and net positive and negative charges are produced in two opposite faces.

On the contrary, if an alternating voltage is applied to two opposite faces of a piece of crystal, it mechanically vibrates. The vibration of crystal with applied voltage is called ***reverse piezoelectric effect***. The vibration is the so-called thickness-shear or face-shear vibration, in which both surfaces of the crystal plate shift w.r.t. each other as shown in Fig.8-10.

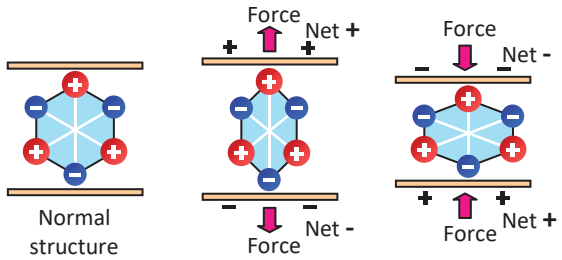


Fig.8-9: Piezoelectric effect

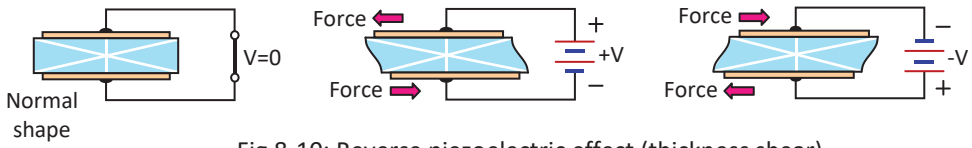


Fig.8-10: Reverse piezoelectric effect (thickness shear)

Quartz is mostly used as a piezoelectric material. Quartz is a hard, crystalline mineral composed of silicon and oxygen atoms (SiO_4). As natural quartz is costly to mine, most of the quartz used for crystal fabrication today is of the ***cultured*** or ***synthetic*** variety. To make the device (resonator), quartz crystal is cut in different orientations and thickness as shown in Fig.8-11. After cutting, the piece of crystal is placed between two conducting plates that work as the

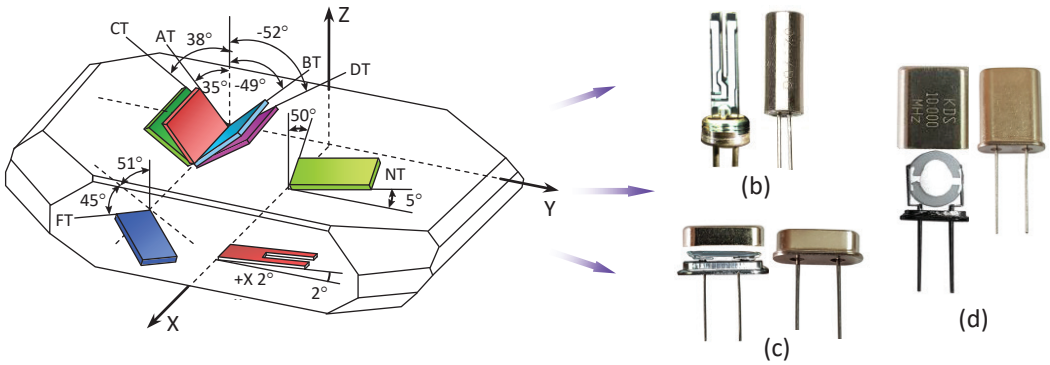


Fig.8-11: (a) Different cutting angles of quartz crystal (b) Crystals used in watch, (c) Small crystal used in microprocessor, and (d) Big crystals used in microprocessor or other purposes

external electrodes of the crystal. The assembly is placed in a metal case. The frequency of oscillation is determined by the type of cut, cutting angle, dimensions of the crystal piece, and construction of the electrodes.

8.10 Quartz Crystal Equivalent Model and Response

A mechanically vibrating crystal can be represented by an equivalent electrical circuit consisting of a low value ***motional resistance*** R_s ($10\ \Omega$ to $150\ \Omega$), a large ***motional inductance*** L_s (few mH to H) and small motional capacitance C_s (2 fF to 50 fF) as shown in Fig.8-12(b). As the crystal is placed in between two metal plates, they form a capacitance which is represented by C_m, and is called ***mounting capacitance***. Its value ranges from 0.5 pF to 10 pF. When a crystal vibrates, its inertia is equivalent to L_s, stiffness is equivalent to C_s and frictional loss is equivalent to R_s. The quality factor (Q) of an inductor is defined as $2\pi L/R$. The value of R in a crystal is so small that it can give quality factor in the range of 10^4 to 10^6, while the quality factor of a very good inductor is 10^3. For the very high value of quality factor the stability of a crystal oscillator is very high.

The impedance vs. frequency graph of a typical crystal is shown in Fig.8-12(c).

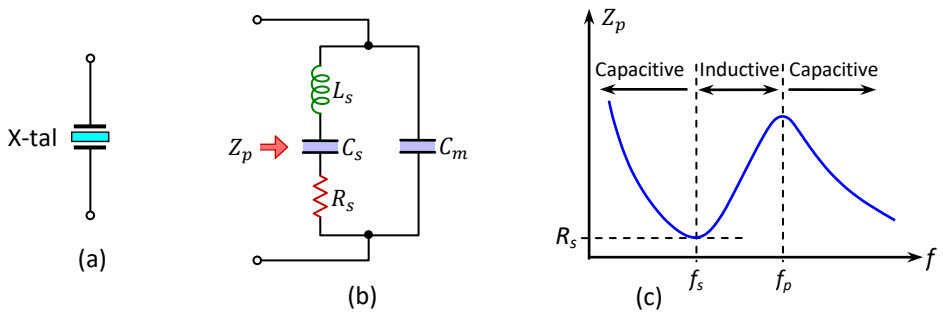


Fig.8-12: (a) Symbol of crystal, (b) Equivalent circuit, and (c) Characteristics

From the equivalent model of the crystal [Fig.8-12(b)], its impedance can be represented as,

$$or, \quad Z_p = \left(\frac{j}{\omega}\right) \times \frac{(\omega^2 L_s C_s - 1)}{C_s + C_m - \omega^2 L_s C_s C_m} \tag{8-10}$$

From this equation we find that Z_p depends on frequency (ω). $Z_p = 0$, when $\omega^2 L_s C_s - 1 = 0$. This is the condition of series resonance. Therefore, at series resonance,

$$\omega_s^2 L_s C_s - 1 = 0$$

$$or, \quad f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{8-11}$$

Series resonance occurs at lower frequency at which the mounting capacitance has negligible effect.

In case of parallel resonance, $Z_p = \infty$ when $C_s + C_m - \omega^2 L_s C_s C_m = 0$. Therefore, at parallel resonance,

$$C_s + C_m - \omega_p^2 L_s C_s C_m = 0$$

or,
$$\omega_p^2 = \frac{C_s + C_m}{L_s C_s C_m} = \frac{1}{L_s C_T}$$

where, $C_T = C_s C_m/(C_s + C_m) = C_s \| C_m$.

or,
$$f_p = \frac{1}{2\pi\sqrt{L_s C_T}} \tag{8-12}$$

Quality Factor or *Q*-factor:

Quality factor or Q-factor (Q) of a crystal or (coil) is defined as the ratio of the maximum energy stored to the maximum energy dissipated per cycle of the resonant frequency. It can be shown that

$$Q = 2\pi f \frac{\text{maximum energy stored}}{\text{maximum energy dissipated}} = \frac{X_L}{R} = \frac{2\pi f L_s}{R} \tag{8-13}$$

Since the value L_s of a crystal is very large and R is very small, the quality factor of a crystal is very large.

8.11 Colpitts Oscillator with Crystal

In Colpitts oscillator, the capacitors and the inductor jointly determine the frequency of oscillation. As the Q-factor of a coil is low, the frequency of Colpitts oscillator drifts due the variation of temperature or external magnetic fields. In place of inductor, if a crystal is used more stable frequency is obtained. In this case, the equivalent inductance of the crystal forms the tank circuit and determines the frequency of oscillation. We can replace the inductor of Fig.8-6 by a crystal of desired frequency. However, generally Colpitts crystal oscillators are designed using a common collector amplifier as shown in Fig.8-13(a). In this circuit, the crystal works as an inductor and produces a frequency little greater than its series resonant frequency (f_s). A damped oscillation is produced in the tank circuit consisting of the crystal's inductance and the capacitors C_1 and C_2. The output voltage is applied across C_2 and the feedback voltage is taken from across capacitors $C_1 + C_2$. Look, the polarity of the output voltage and the feedback voltage are same. The CC amplifier produces no phase shift, so the total phase shift of the oscillator is 0°.

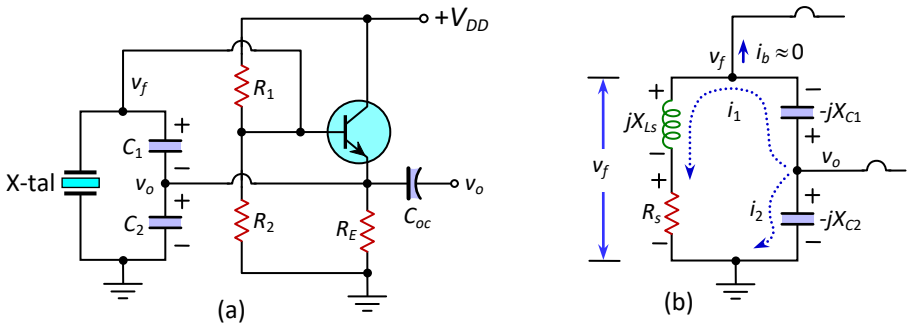


Fig.8-13: (a) Crystal Colpitts oscillator using CC amplifier, (b) Current direction in the tank circuit

The gain of the CC amplifier is less than unity. So the value of the feedback factor (β) should be greater than unity. From Fig.8-13(b), the voltage across, C_1 and C_2 is the feedback voltage, v_f. Similarly the voltage across C_2 is the output voltage, v_o. Here, C_1 and C_2 forms a voltage divider network. According to voltage divider rule we can write,

$$v_o = \frac{v_f X_{C2}}{jX_{C1} + jX_{C2}}$$

$$\beta = \frac{v_f}{v_o} = \frac{X_{C1} + X_{C2}}{X_{C2}} = 1 + \frac{X_{C1}}{X_{C2}} = 1 + \frac{C_2}{C_1} \qquad (8\text{-}14)$$

From this expression, we find that β increases with the increase of C_2 and decrease of C_1.

8.12 Pierce Crystal Oscillator

Pierce crystal oscillator is a modification of Colpitts oscillator. Here the inductor of Colpitts oscillator has been replaced by a crystal (a frequency generating device made of quartz crystal). The pierce crystal oscillator is shown in Fig.8-14(a). The feedback process is illustrated in Fig.8-14(b).

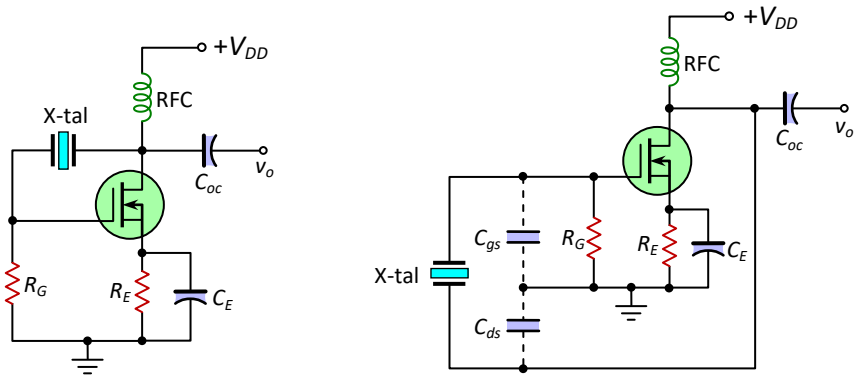


Fig.8-14: Pierce crystal oscillator (a) Normal circuit, and (b) Circuit with FET junction capacitances

The gate-source capacitance (C_{gs}) and the drain-source capacitance (C_{ds}) come across the crystal. A crystal can work either in series or in parallel resonance mode. In this circuit, the crystal works in series resonance mode. In series resonance the crystal is equivalent to an inductor. This inductance of the crystal, and the parasitic capacitances of the FET from a tank circuit. Rest of the operation is same as the Colpitts oscillator.

8.13 Multivibrator

A ***multivibrator*** is an electronic circuit that produces a non-sinusoidal (square) waveforms as its output. There are three types of multivibrators:

- Astable Multivibrator
- Monostable Multivibrator
- Bistable Multivibrator

8.14 Astable Multivibrator

The ***Astable Multivibrator*** is one type of cross-coupled transistor switching circuit that has NO stable output state, as it changes from one state to another (HIGH and LOW) by its own. That is, the output of this circuit (taken from the collector terminal of any transistor) freely oscillates between HIGH and LOW state [as shown in Fig.8-15(b)]. The astable multivibrator is also called free running multivibrator.

As shown in Fig.8-15(a), an astable multivibrator is consisted of two transistors, two capacitors and four resistors.

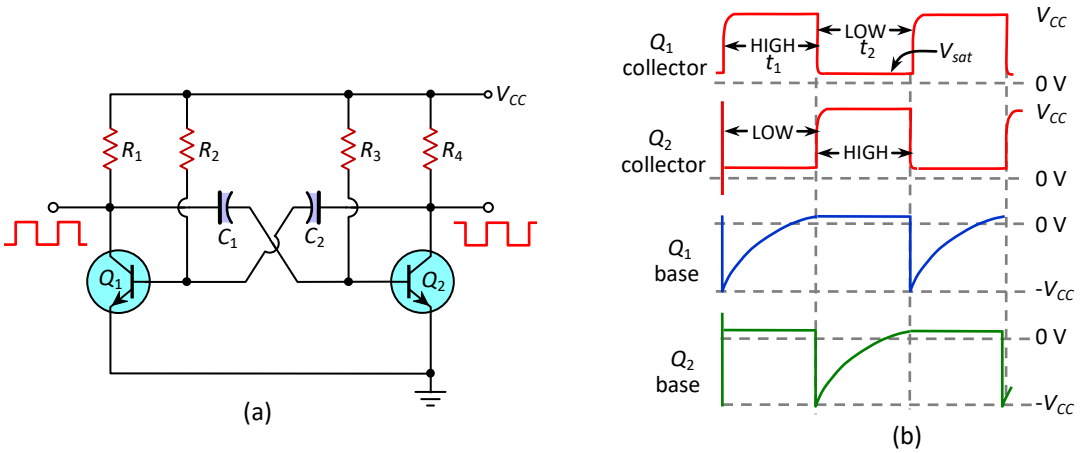


Fig.8-15: Astable multivibrator: (a) Schematic diagram, and (b) Output waveforms

The HIGH and LOW time depends on the values of R_2, R_3, C_1, and C_2 as given by the following expressions:

HIGH Time : $t_1 = 0.69\ C_1\ R_3$

LOW Time : $t_2 = 0.69\ C_2\ R_2$

Time period : $T = t_1 + t_2 = 0.69\ C_1\ R_3 + 0.69\ C_2\ R_2$

If $R_2 = R_3 = R$, and $C_2 = C_3 = C$

Then, $T = 1.38\ RC$. Therefore, the frequency of oscillation will be,

$$f = \frac{1}{0.69(C_1\ R_3\ + C_2\ R_2)} = \frac{1}{1.38\ RC}$$

8.15 Monostable Multivibrator

The circuit diagram of a monostable multivibrator is shown in Fig.8-16(a). As shown in Fig.8-16(b), the output of this multivibrator has a stable state and a quasi-stable state. The output goes to quasi-stable state when a trigger pulse is applied to the base of any transistor. The duration of the quasi-stable state will be: $T = 0.693 R_T C$. After this time the output backs to the stable stage, and stays there until the next trigger pulse is applied.

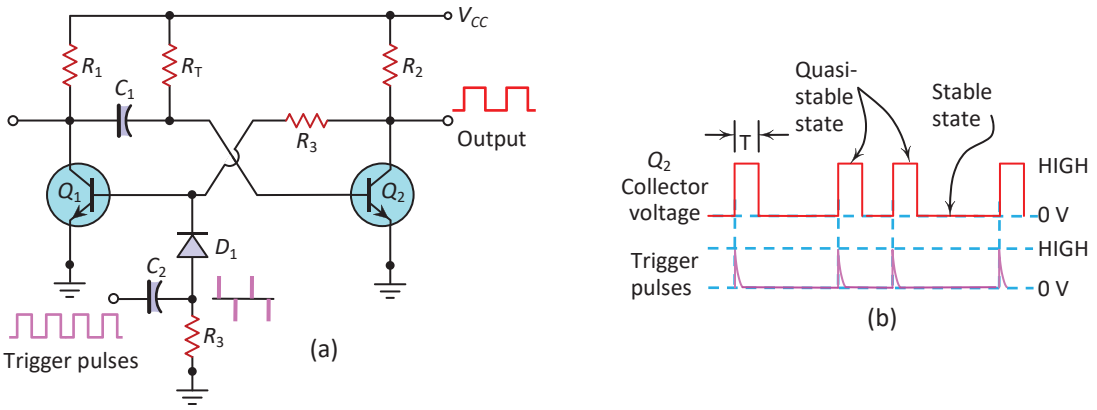


Fig.8-16: Monostable multivibrator: (a) Schematic diagram, and (b) Output waveforms

8.16 Bistable Multivibrator

A bitable multivibrator has 2 stable states. The output goes to HIGH state at one trigger pulse, and goes to LOW state at another trigger pulse and so on [as shown in Fig.8-12].

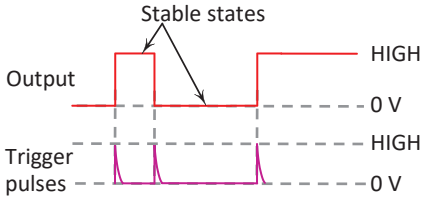
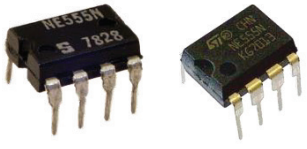


Fig.8-17: Output of bistable multivibrator

8.17 The Timer IC: 555

The ***555 timer*** is a commonly used IC, designed to produce a variety of output waveforms with the addition of an external *RC* network. Using this IC, different types of multivibrators can be designed.



(a)

(b)

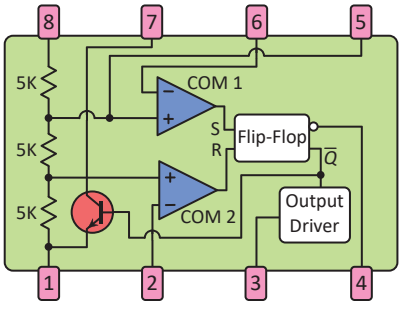


Fig.8-18: The 555 (timer) IC: (a) Photographs, and (b) Internal block diagram

8.18 Astable Multivibrator using 555 IC

The circuit diagram of an astable multivibrator using 555 timer is shown in Fig.8-19. The durations of HIGH and LOW times are controlled by two resistors R_1, R_2 and one capacitor C_1.

HIGH time: $t_1 = 0.69\ (R_1 + R_2)C_1$

LOW time: $t_2 = 0.69\ R_2C_1$

Time period : $T = t_1 + t_2 = 0.69\,(R_1 + R_2)C_1 + 0.69\,R_2C_1 = 0.69\,(R_1 + 2R_2)C_1$.

Therefore, the frequency of oscillation will be,

$$f = \frac{1}{T} = \frac{1}{0.69(\,R_1\, +\, 2R_2)C_1}$$

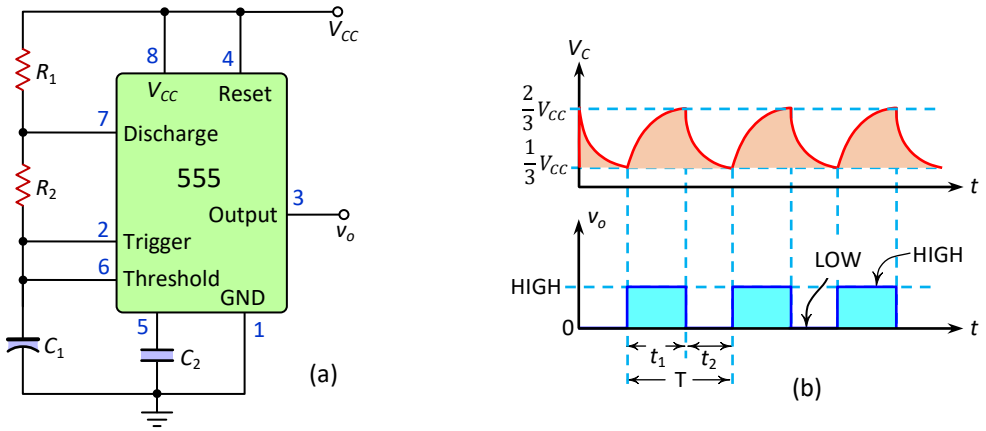


Fig.8-19: Astable multivibrator using 555 IC: (a) Schematic diagram, and (b) Output waveforms

8.19 Monostable Multivibrator

The output of this multivibrator has a stable state and a quasi-stable state. As shown in Fig.8-20(b), the stable state is LOW and the quasi-stable state is HIGH. The output goes to the quasi-stable state when a trigger pulse is applied. After some time the output comes back to the stable stage, and stay there until the next trigger pulse is applied. Unlike the BJT monostable multivibrators, here a negative trigger pulse (less than $1/3$ of V_{CC}) is used. Monostable multivibrator is used to turn-ON a load (like a microwave oven) for a predefined amount of time and let it turn-OFF automatically.

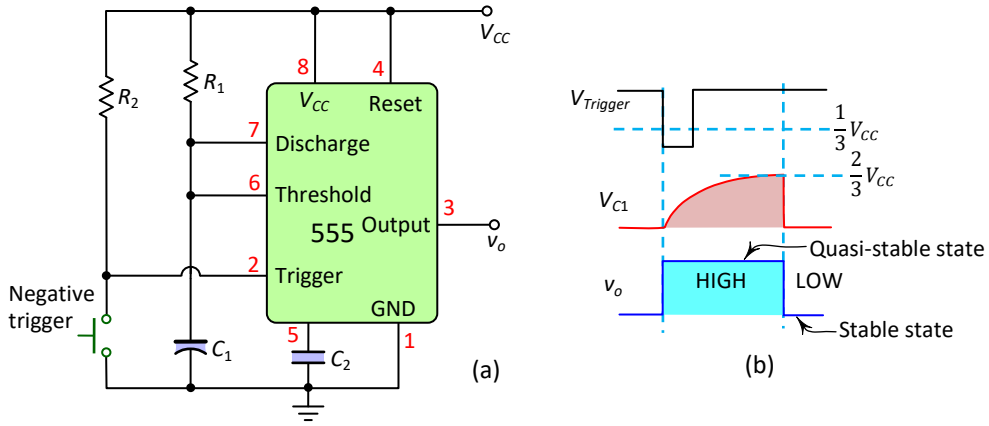


Fig.8-20: Monostable multivibrator using 555: (a) Schematic diagram, and (b) Output waveforms

CHAPTER

9

Regulated Power Supply

9.1 Power Supply Characteristics

A power supply is a circuit that converts AC power into DC at a desired voltage level (5 V, 6 V, 12 V, etc.). In many electronic systems, like mobile, TV, sound system etc. we use power supply. Fig.9-1 shows an unregulated power supply that consists of a step-down transformer (T_1), a bridge rectifier (consists of D_1 to D_4) and a capacitor filter (C_1). A problem of this power supply is due to the variation of supply voltage or the load current, the output voltage changes. Due to the internal voltage drop, an increase in load current always decreases the load voltage. Therefore, voltage regulators are used to regulate (keep constant) the output voltage. The performance of a voltage regulator is determined by two parameters: ***load regulation*** and ***line regulation***.

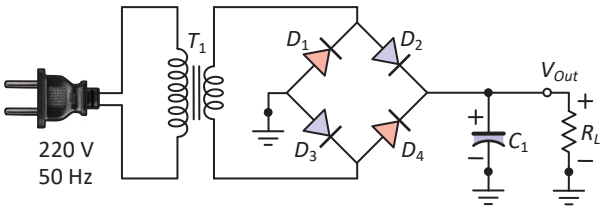


Fig.9-1: Unregulated power supply with capacitor filter

Load Regulation

When the amount of current through a load changes due to variations in load resistance, the voltage regulator must maintain a nearly constant output voltage across the load, as illustrated in Fig.9-2.

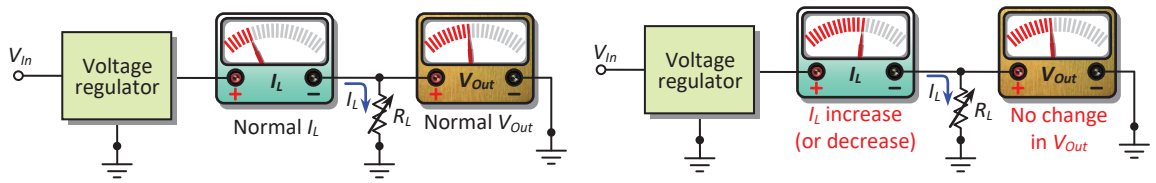


Fig.9-2: Load regulation. A change in load current has practically no effect on the output voltage of a regulator (within certain limits)

Load regulation can be defined as the percentage change in output voltage for a given change in load current with all other factors held constant. One way to express load regulation is as a percentage change in output voltage from no-load (NL) to full-load (FL). Mathematically,

$$\text{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}}\right) \times 100\% \qquad (9\text{-}1)$$

Alternately, the load regulation can be expressed as a percentage change in output voltage for each mA change in load current. For example, a load regulation of $0.01\%/\text{mA}$ means that the output voltage changes (increase or decrease) by 0.01% when the load current increases or decreases by $1\ \text{mA}$.

Example 9-1

A certain voltage regulator has $12\ \text{V}$ output when there is no load ($I_L = 0$). When the full-load current of $200\ \text{mA}$ is drawn from the regulator, the output voltage falls to $11.8\ \text{V}$. Calculate the voltage regulation as a percentage change from no-load to full-load and also as a percentage change for each mA change in load current.

Solution:

Here, the no-load voltage is $V_{\text{NL}} = 12\ \text{V}$, and the full-load voltage is $V_{\text{NL}} = 11.8\ \text{V}$. The voltage regulation (load regulation) can be calculated using Equ.(9-1) as,

$$\text{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}}\right) \times 100\% = \left(\frac{12\ \text{V} - 11.8\ \text{V}}{11.8\ \text{V}}\right) \times 100\%$$

$$\therefore \quad \text{Load regulation} \approx 1.7\%\ [\text{Ans.}]$$

The load regulation can also be calculated as a percentage change per mA of output current as,

$$\text{Load regulation} = \frac{1.7\%}{200\ \text{mA}} \approx 0.0085\%/\text{mA}\ [\text{Ans.}]$$

Comments: The smaller the load regulation, the better the power supply.

Line Regulation

The ability of a regulator to maintain a constant voltage irrespective of the input (supply) voltage change is measured by ***line regulation***. Line regulation can be defined as the percentage change

in the output voltage for a given change in the input voltage (generally 10%) with all other factors held constant. It is also expressed as a percentage by the following formula:

$$\text{Line regulation} = \left(\frac{\Delta V_{Out}}{\Delta V_{in}}\right) \times 100\% \qquad (9\text{-}2)$$

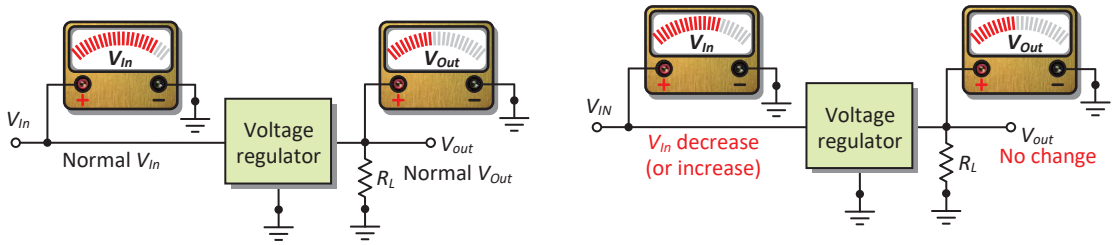


Fig.9-3: Line regulation. A change in input (line) voltage does not significantly affect the output voltage of a regulator (within certain limits)

Line regulation can also be expressed in units of %/V. For example, a line regulation of 0.05%/V means that the output voltage changes by 0.05% when the input voltage increases or decreases by one volt. Line regulation can also be calculated using the following formula (Δ means *a change*):

$$\text{Line regulation} = \left(\frac{\Delta V_{Out}/V_{Out}}{\Delta V_{in}}\right) \times 100\% \qquad (9\text{-}3)$$

Example 9-2

Due to the decrease in the AC input voltage of a certain power supply, the DC input to the voltage regulator decreases by 5 V, and the output of the regulator decreases by 0.25 V. The nominal output is 12 V. Determine the line regulation in %/V.

Solution:

Using Equ.(9-3), $\text{Line regulation} = \left(\frac{\Delta V_{Out}/V_{Out}}{\Delta V_{in}}\right) \times 100\%$

or, $\text{Line regulation} = \left(\frac{0.25\text{ V}/12\text{ V}}{5\text{ V}}\right) \times 100\% \approx 0.42\%/\text{V}$ [Ans.]

Comments: The lower the value of line regulation the better the regulator quality.

9.2 Types of Voltage Regulator

There are mainly two types of voltage regulators: ***linear voltage regulator*** and ***switching*** or ***switch mode voltage regulator***. Though both types regulate a system's voltage, but linear regulators operate with lower efficiency and switching regulators operate with higher efficiency. In high-efficiency switching regulators, most of the input power is transferred to the output without losses.

9.2.1 Linear Regulators

A linear voltage regulator utilizes an active pass device (or controlling device) (such as BJTs or MOSFETs), which is controlled by a high-gain (BJT or op-amp) amplifier. To maintain a constant output voltage, the linear regulator adjusts voltage dropped in the pass device by comparing the internal voltage reference to the sampled output voltage, and then adjusts the error to zero. Linear regulators are step-down converters, so the output voltage is always lower the input voltage.

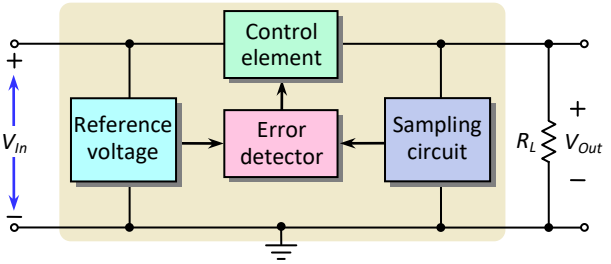


Fig.9-4: Block diagram of a series type voltage regulator

Linear regulator ICs, such as the 78xx, only require an input and output capacitor to operate (see Fig.9-11). Their simplicity and reliability make them very simple devices for engineers, and are often highly cost-effective.

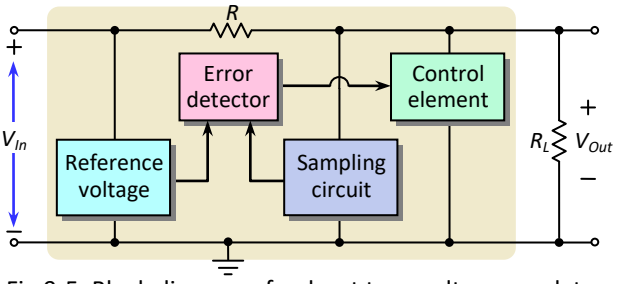


Fig.9-5: Block diagram of a shunt type voltage regulator

Two basic types of linear regulators are the ***series regulator*** and the ***shunt regulator***. If the controlling device (BJTs or MOSFETs) is connected in series with the load, then it is called a series regulator, but if the controlling device is connected in parallel (shunt) with the load then it is called shunt regulator. The block diagram of a series and a shunt regulator is given in Fig.9-4 and Fig.9-5, respectively.

9.2.2 A Switching Regulator

A switching regulator circuit is generally more complicated than a linear regulator, and requires many electronic components. Switching regulators can be step-down converters, step-up converters, or a combination of the two, which makes them more versatile than a linear regulator. The block diagram of a switching regulator is shown in Fig.9-6. The unregulated voltage is chopped with high frequency and then transferred to a higher or lower voltage using transformer. At the output, this AC voltage is rectified and filtered and the output voltage is produced. The output voltage is kept constant by changing the width (PWM: Pulse Width Modulation) of the chopping

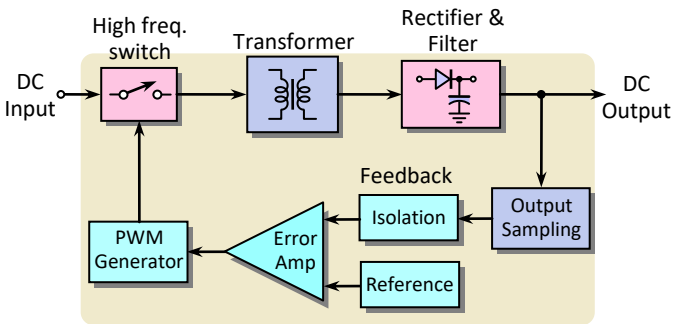


Fig.9-6: Block diagram of a switching type voltage regulator

signal. Advantages of switching regulators are: they are highly efficient (greater than 95%), have better thermal stability, and can support higher current and wider V_i/V_o applications. The HF920 is an example of a switching regulator that offers high reliability and efficient power regulation. A complete power supply with switching regulator is called ***switch mode power supply*** or SMPS.

Basic Circuit of Linear Series Regulator

In Chapter 2, we have discussed a basic voltage regulator (shunt type) using Zener diode. In that type of regulator, the load current is limited by the maximum Zener diode current capacity.

The current capacity can be increased by using a series-pass transistor as shown in Fig.9-7. This circuit is a ***series voltage regulator***. Transistor Q_1 is reffered to a ***series-pass transistor***.

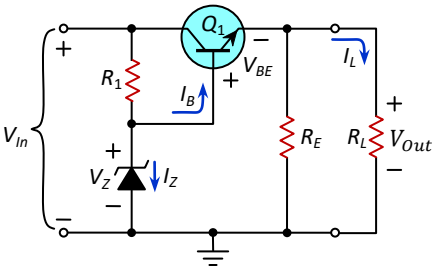


Fig.9-7: Block diagram of a series type voltage regulator

The output voltage (V_{Out}) of this regulator is ($V_Z - V_{BE}$), and the maximum load current $I_{L(max)}$, can be the maximum emitter current of Q_1. For a 2N3055 transistor, I_L can be as much as 15 A.

9.3 Regulator With Error Amplifier

A series regulator with an ***error amplifier*** is shown in Fig.9-8. The error amplifier improves the line regulation and load regulation. The amplifier also makes it possible to have an output voltage greater than the Zener diode voltage. Resistor R_2 and Zener dicde D_1 produce the reference voltage (V_Z). Transistor Q_2 and R_1 constitute the error amplifier, that controls the series-pass transistor Q_1. The output voltage is divided by R_3, and R_4 resistors and compared to the reference voltage. C_1 is a large value capacitor, usually 50 µF to 100 µF, used to suppress any oscillations at the output.

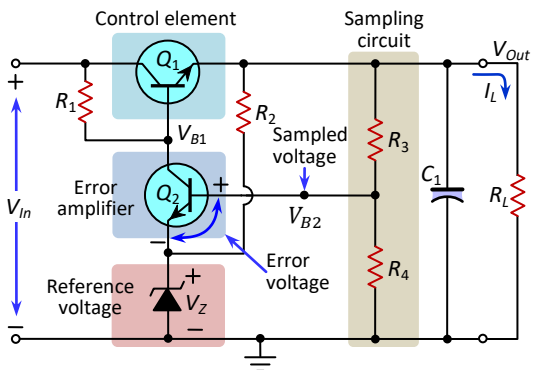


Fig.9-8: Block diagram of a series type voltage regulator

When the circuit output voltage changes, the change is amplified by transistor Q_2 and fed back to the base of Q_1 to correct the output voltage level. Suppose that the circuit is designed for $V_{Out} = 12$ V. The supply voltage (V_{In}) should be greater than V_{Out}, say $V_{In} = 18$ V. Let, $V_Z = 6$ V. The base voltage of Q_2 must be, $V_{B2} = V_Z + V_{BE2} = 6.7$ V. Resistors R_3 and R_4 will divide $V_{Out}(= 12$ V) and produce $V_{B2} = 6.7$ V. The voltage at the base of Q_1 is, $V_{B1} = V_{Out} + V_{BE1} = 12.7$ V. Also, $V_{R1} = V_{In} - V_{B1} = 5.3$ V.

Now suppose (for any reason) the output voltage drops slightly. When V_{Out} drops, V_{B2} also drops. As the emitter voltage of Q_2 is held at V_Z, any decrease in V_{B2}, appears across the base-emitter of Q_2. A reduction in V_{BE2} causes I_{C2} to be reduced. When I_{C2} falls, the voltage drop across R_1 also drops. So the voltage at the base of Q_1 rises ($V_{B1} = V_{In} - V_{R1}$) causing the output

voltage to increase. Thus, a decrease in V_{Out} produces a feedback effect which causes V_{Out} to increase back to its normal level. In the same process, a rise in V_{Out} above its normal level produces a feedback effect which pushes V_{Out} down again to its normal level.

9.4 Three-Terminal Voltage Regulator ICs

The 78xx is a family of self-contained voltage regulator integrated circuits (ICs) used for positive voltage. On the other hand, 79xx series are used for negative output voltage. As shown in Fig.9-9 and Fig.9-10, the ICs have three terminals. For both the series, xx is a two digit number that represents the value of constant output regulated voltage. For example, 7805 is a voltage regulator IC that produces constant +5 V, and 7905 is the complementary ICs that gives constant -5 V (negative 5 Volts) output. They are capable of providing 1 A output current. They have internal short-circuit protection and thermal protection. As they produce a high power loss, they must be placed in heat-sinks.

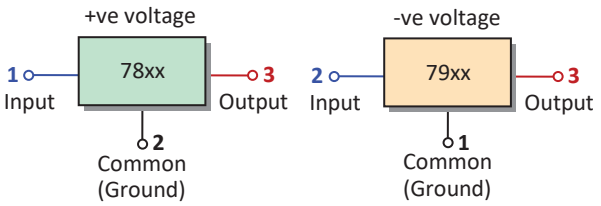


Fig.9-9: **78xx** and **79xx** IC pin-outs

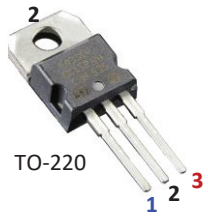


Fig.9-10: Pin-out of 78xx IC

Using these ICs, we can design DC power supply for constant output voltage. Fig.9-11 shows how to use a 7812 IC to produce constant 12 V output. The purpose of the capacitors is to filter any spike voltages. The input voltage should be at least 1 V greater than the output voltage. The output will be constant 12 V. The additional voltage will be dropped across the IC.

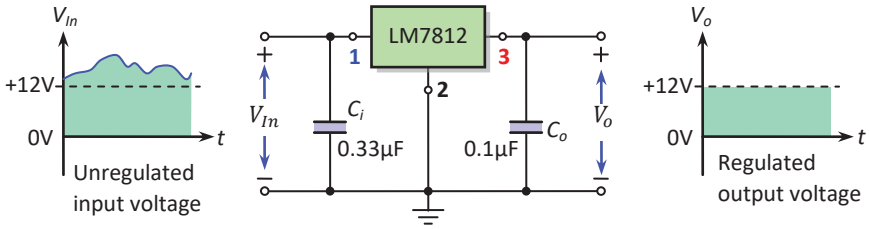


Fig.9-11: Voltage regulator circuit using LM7812 IC for 12 V output

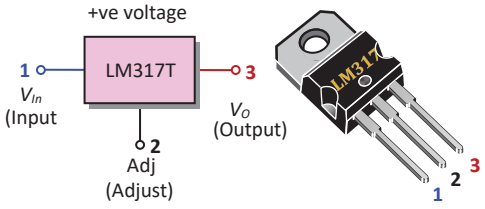


Fig.9-12: Variable voltage IC: LM 317 T

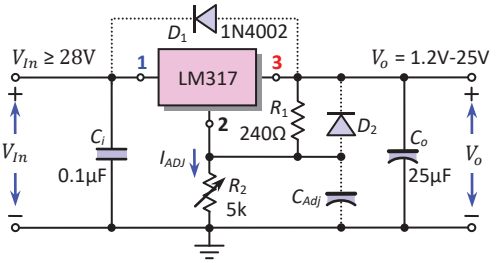


Fig.9-13: Variable voltage regulator circuit

CHAPTER

10

Power Electronics

10.1 Introduction

Power electronics is the branch of electrical engineering that deals with the processing of high voltages and currents to deliver power to different output loads. Some examples of power electronic systems are:

- DC/DC converters
- Light dimmer / Fan regulator circuits
- Inverter circuits etc.

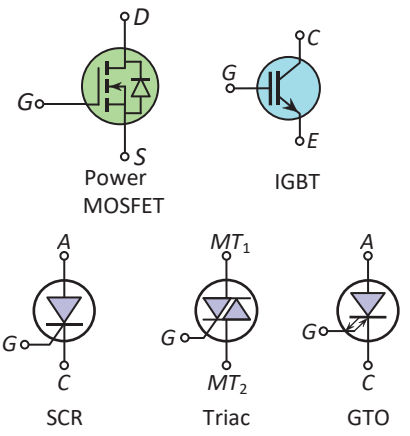


Fig.10-1: Symbols of some common power devices

10.2 Devices Used in Power Electronics

Power electronic circuits are designed using different power devices, depending on the power requirements and some other parameters. Some common components used in power electronics are:

- Power BJT
- Power MOSFET
- IGBT (insulated-gate bipolar transistor)

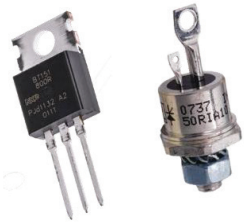


Fig.10-2: Photographs of typical SCRs

- SCR (Silicon-controlled rectifier)
- Triac
- GTO (gate turn-off thyristor)

10.3 SCR (Silicon Controlled Rectifier)

SCR is a high power silicon device. It is a four layer PNPN device. As it is made using Si, and the device controls power, so it is called ***silicon controlled rectifier*** (***SCR***).

The *I-V* characteristics of an SCR ae given in Fig.10-3. If an SCR is reverse biased, it will behave as an open switch and will flow a very small reverse leakage current. If the reverse bias voltage exceeds V_{RB} (reverse break down voltage), the device will be damaged and unlimited current will flow through it. If the SCR is forward biased and the applied voltage is equal to V_{BO}, the SCR turns ON and starts to conduct current (ON switch). When turns ON its internal resistance decreases, and hence the voltage drop decreases as well. As shown in Fig.10-3, if a gate current is applied, SCR turns ON with lower forward bias voltage.

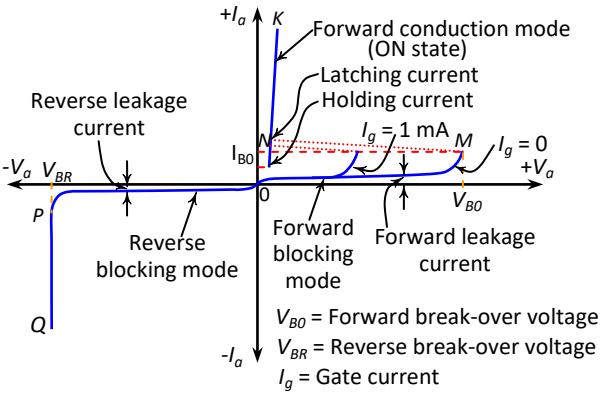


Fig.10-3: Characteristics of SCR

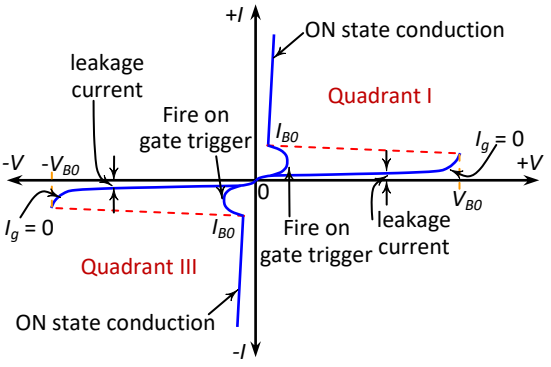


Fig.10-4: Characteristics of Triac

10.4 The Traic

The characteristics of a triac is shown in Fig.10-4. Triac is also a power device that is used for AC power controlling. Its characteristics are similar to those of SCR. The only difference is, it works in both directions: forward bias and reverse bias. So it can be used for AC power controlling.

10.5 The IGBT

IGBT is the short form of ***Insulated Gate Bipolar Transistor***, combination of Bipolar Junction Transistor (BJT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). As shown in Fig.10-6(a), it is the combination of a MOSFET and a BJT. It is a semiconductor device used as very high power switch.

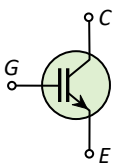


Fig.10-5: Symbol of IGBT

MOSFET has advantages of high switching speed with high input-impedance and on the other side BJT has advantage of high gain and low voltage drop. As IGBT is a combination of MOSFET and BJT, it has advantages of both of them. Although, BJT is current controlled device but the control for the IGBT depends on the MOSFET, thus it can be considered as a voltage controlled device. The

input characteristic is same as that of EMOSFET and the output characteristics are same as that of BJT [as shown in Fig.10-6(b) and (c)].

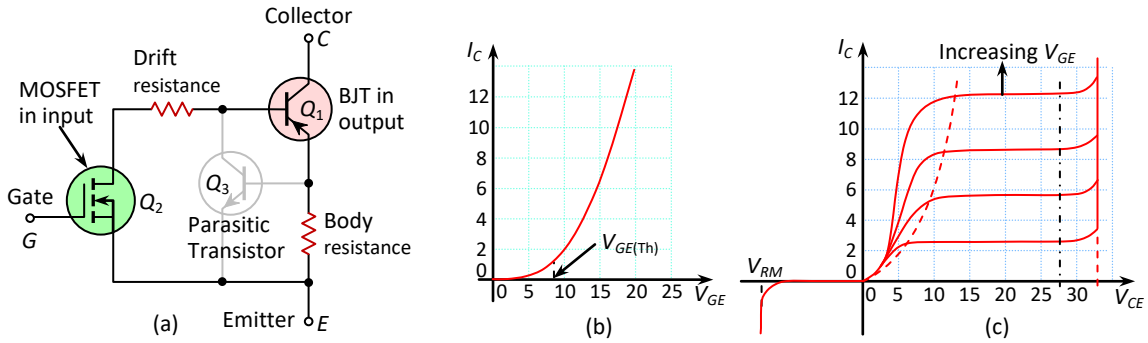


Fig.10-6: (a) Equivalent circuit of IGBT, (b) Input characteristics, and (c) Output characteristics

10.6 Power MOSFET

There are various types of Power MOSFET. The most common types are: VMOS, and UMOS. The construction of a VMOS is shown in Fig.10-7. Here, the channel length can be controlled by diffusion process and can be made very thin to carry large current.

The structure is same as an N-channel enhancement MOSFET. Therefore, its operation and characteristic curves are similar to that of N-channel enhancement MOSFET. The only difference is now the devices can carry a very large current.

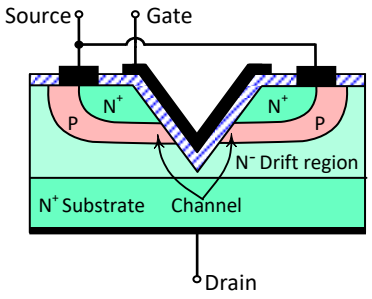


Fig.10-7: Construction of V-MOS

10.7 DC-to-DC Converter

DC-to-DC converters are used to convert a DC input voltage into a higher or lower DC output voltage. There are three types of DC-to-DC converters:

- Buck converter : Output voltage is less than input voltage.
- Boost converter : Output voltage is greater than input voltage.
- Buck-Boost converter : Output voltage may be less than or greater than input voltage.

DC-to-DC Converter Circuit

The circuit diagram of a buck-boost converter is shown in Fig.10-8. The output is controlled by changing the duty cycle of a PWM (pulse width modulation) signal. The definition of duty-cycle is given in Fig.10-9. If the duty-cycle of the controlling pulses is changed to increase or decrease the output voltage, it is called PWM. When the PWM signal is HIGH, the MOSFET is ON and energy is stored in the inductor L_1. At this time, the load is separated from the source by the diode D_1 but the capacitor C_1 supplies power to the load. When PWM goes LOW, the MOSFET is OFF, the

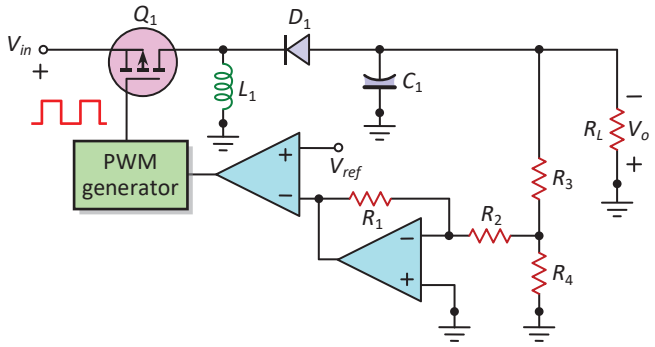


Fig.10-8: Schematic diagram of a DC-to-DC converter

Duty-Cycle (DC):

Duty-cycle of a pulse is defined as:

$$\text{DC} = \frac{\text{HIGH time}}{\text{Period}} \times 100 = \frac{W}{T} \times 100$$

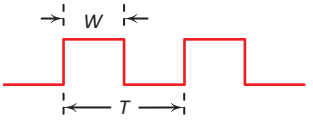


Fig.10-9: Duty-cycle of a pulse train

energy stored in the inductor charges up the capacitor as well as supplies power to the load. By changing the duty cycle, the output voltage can be increased or decreased as given by the following equation.

$$V_o = \frac{DC}{1 - DC} V_{in} \qquad (10\text{-}1)$$

DC-to-DC converters are so widely used in electronics that they are readily available in market as modular froms. Fig.10-10 shows such a DC-to-DC converter module.

Fig.10-10: DC-to-DC converter

10.8 Phase Control Using Triac (Fan Regulator)

It is possible to control the power supplied to a load, using triac and diac. This type of circuit is called phase-controlling circuit. They are widely used as fan-regulators and light-dimmers in our homes. A typical circuit diagram of a fan- regulator (and light-dimmer) circuit is shown in Fig.10-11. The power, supplied to the load, is controlled by changing the firing position (also called triggering angle, α) of the diac and triac on each cycle of the AC input power as shown in Fig.10-12. The triggering angle (α) can be changed by changing the value of the resistance VR_1. The higher the value of α, the lower is the power supplied to the load.

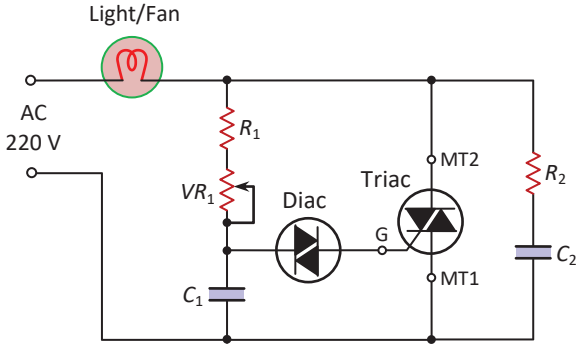


Fig.10-11: Phase control circuit using diac and triac

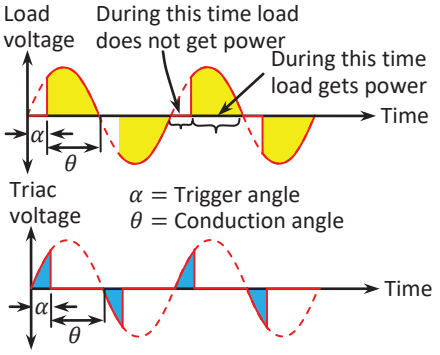


Fig.10-12: The load and triac voltages

CHAPTER 11

Digital Electronics

11.1 Introduction

Our universe is analog in nature. Maximum parameters (measureable quantities) surrounding us are analog, for example, time, temperature, wind speed, pressure, force and so on. These analog quantities have an important characteristic: they can vary over a continuous range of values. If we measure room temperature, it may have any value between 0℃ to say 40℃, or if we measure wind speed it may have any value between 0 to 200 km/hour.

In digital systems, these analog quantities are represented by digital signals. Digital signals are not continuous rather discrete and these discrete values are represented by binary numbers. Binary numbers are the combination of '0' and '1'.

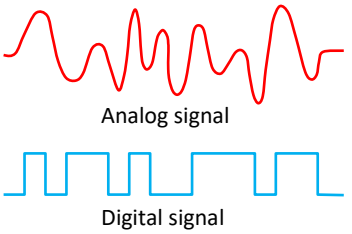


Fig.11-1: Analog and digital signals

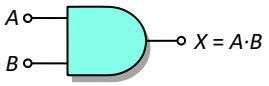
A circuit that processes digital signal is called ***digital circuit***. The branch of electronics in which digital circuits are studied is called ***digital electronics***. In digital circuits '0' and '1' are represented by high voltage and low voltage, respectively. The major difference between analog and digital quantities, then, can be simply stated as follows: ***analog*** = ***continuous*** and ***digital*** = ***discrete*** (step by step).

Because of the discrete nature of digital representation, it is more immune to noise, whereas the analog quantity is noise prone.

11.2 Logic Gates

Analog circuits are constructed using discrete components and ICs, but the building blocks of digital circuits are ***logic gates***. They perform basic logical functions that are fundamental to digital circuits.

In a digital circuit, logic gates will make decisions based on a combination of digital signals applied to its inputs. Though logic gates may have more than two inputs, most of them have two inputs and one output. Logic gates work based on ***Boolean algebra*** (the algebra where the variables have values either 0 or 1). At any given time, every terminal of logic gates is in one of the two binary conditions, **FALSE** (0) or **TRUE** (1). FALSE represents 0, and TRUE represents 1. A logic gate can be thought of like a switch, where one position of the output is OFF ('0'), and the other position is ON ('1'). Logic gates are commonly used in integrated circuits (IC). In fact, logic gates are constructed using analog devices, like resistors, diodes, transistors etc. There are three fundamental logic gates and combining these gates some other logic gates are made. Sometimes to describe the function of a logic gate or a digital circuit, ***truth table*** is used. A ***truth table*** is a means for describing how a logic gate's (or circuit's) output depends on the input logic levels.

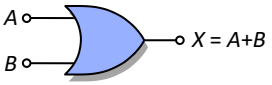


AND gate

Truth table of AND gate

Input		Output
A	***B***	***X = A·B***
0	0	0
0	1	0
1	0	0
1	1	1

Fig.11-2: Symbol and truth table of an AND gate



OR gate

Truth table of OR gate

Input		Output
A	***B***	***X = A+B***
0	0	0
0	1	1
1	0	1
1	1	1

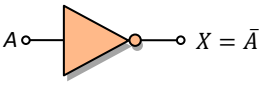
Fig.11-3: Symbol and truth table of an OR gate

The AND Gate

The ***AND gate*** acts in the same way as the logical "and" operation. The symbol of a two-input AND gate and its truth table are shown in Fig.11-2. The output of an AND gate will be '1' if both the inputs are '1'. If the value of any input is '0', the output will be '0'. In Boolean algebra the AND operation is denoted by . (dot). So the output of the AND gate can be represented as $X = A \cdot B$. Sometimes, the 'dot' is not used and the operation is simply denoted as $X = AB$.

The OR Gate

The ***OR gate*** acts in the same way as the logical "or" operation. The symbol of a two-input OR gate and its truth table are shown in Fig.11-3. The output of an OR gate will be '1' if any one of the inputs is '1'. If the values of all inputs are '0', the output will be '0'. In Boolean algebra the OR operation is denoted by + (plus) sign as shown in Fig.11-3. So the output of the OR gate can be represented as $X = A + B$.



NOT gate

Truth table of NOT gate

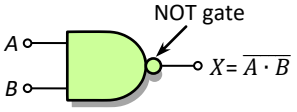
Input	Output
A	***X*** = $\bar{A}$
0	1
1	0

Fig.11-4: Symbol and truth table of a NOT gate

The NOT Gate

A ***NOT gate***, also called a logical ***inverter***, has only one input. It produces reverse of the input. If the input is '1', then the output is '0'. If the input is '0', then the output is '1'. The symbol and the truth table of a NOT gate are shown in Fig.11-4. In Boolean algebra, the NOT operation is denoted by ¯ (over bar) symbol. So the output of the NOT gate can be represented as $X = \bar{A}$

All digital circuits can be constructed using the above mentioned three logic gates. For this reason they are called ***fundamental logic gates***. Combining the NOT gate with the AND and OR gates, two more gates are produced. These are NAND and NOR gates.

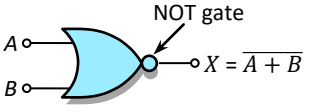


NAND gate

Truth table of NAND gate

Input		Output
A	***B***	***X*** = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Fig.11-5: Symbol and truth table of a NAND gate



NOR gate

Truth table of NOR gate

Input		Output
A	***B***	***X***= $\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Fig.11-6: Symbol and truth table of a NOR gate

The NAND Gate

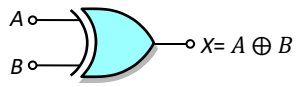
The ***NAND gate*** is the combination of AND gate and NOT gate. The symbol and the truth table of a two-input NAND gate are shown in Fig.11-5. Look at the circle at the output of NAND gate. This circle represents a NOT gate. Thus, the output of a NAND gate will be just opposite of AND gate. The output of a NAND gate will be '1' if any one of the inputs is '0'. The output will be '0', only when all inputs are '1'. In Boolean algebra the NAND operation is denoted by ¯· (dot with over bar) symbol. So the output of the NAND gate can be represented as $X = \overline{A \cdot B}$.

The NOR Gate

The ***NOR gate*** is the combination of OR gate and NOT gate. The symbol and the truth table of a two-input NOR gate are shown in Fig.11-6. Here also the circle at the output indicates a NOT gate. The output of a NOR gate will be just opposite of OR gate. The output will be '0' if any one of the inputs is '1'. The output will be '1', only when all inputs are '0'. The NOR operation is denoted by $\overline{+}$ (plus with over bar) symbol. So the output of the NOR gate will be $X = \overline{A + B}$.

The NAND gates and NOR gates are called ***universal*** gates, as they can be used to build any logical gates or logic circuits.

There are two more logic gates used in digital electronics. These are: *Exclusive-OR* (*Ex-OR*) gate and its complement (inverted) the *Exclusive-NOR* (*Ex-NOR*) Gate. Although they are used as a single building block, they can be constructed using the fundamental gates.

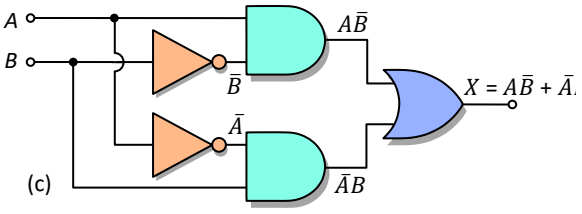


(a) XOR gate

Truth table of XOR gate

(b)

Input		Output
A	***B***	***X = A ⊕ B***
0	0	0
0	1	1
1	0	1
1	1	0

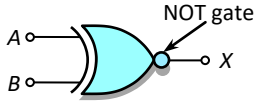


(c)

Fig.11-7: XOR gate: (a) Symbol, (b) truth table, and (c) equivalent circuit of a XOR gate

The Exclusive-OR Gate

XOR **(*Exclusive-OR*)** ***gate*** acts in the same way as the logical "either/or." The output is '1' if either, but not both, of the inputs are '1'. The output is '0' if both inputs are same either '0' or '1'. The symbol and truth table of a two-input XOR gate is given in Fig.11-7. As shown in this figure, the XOR gate can be constructed using the fundamental gates. The XOR operation is denoted by $\oplus$ (circled plus) symbol. So the output of the XOR gate is represented as $X = A \oplus B$.

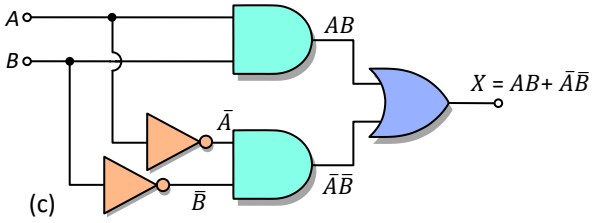


(a) XNOR gate

Truth table of XNOR gate

(b)

Input		Output
A	***B***	***X***
0	0	1
0	1	0
1	0	0
1	1	1



(c)

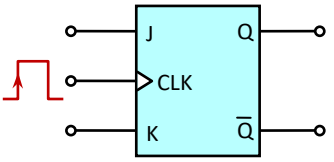
Fig.11-8: XNOR gate: (a) Symbol, (b) truth table, and (c) equivalent circuit of an XNOR gate

The Exclusive-NOR Gate

XNOR (***Exclusive-NOR***) ***gate*** acts just in the opposite way of XOR gate. Actually this gate is the combination of XOR gate and a NOT gate at the output. The symbol and its truth table are given in Fig.11-8. The output is '0' if either, but not both, of the inputs are '1'. The output is '1' if both inputs are same either '0' or '1'. The XNOR operation is denoted by $\overline{\oplus}$ (XOR operation with an over-bar) symbol. So the output of a two-input XNOR gate is represented as $X = \overline{A \oplus B}$. Like the XOR gate, the XNOR gate can be constructed using fundamental gates as shown in Fig.11-8.

Flip-Flops

Digital electronic systems are made using ***combinational circuits*** and ***sequential circuits***. The circuits that have no memory effect, that is, the output depends only on the present values of inputs are called ***combinational logic circuits***. On the other hand, the circuits that have memory effect, that is, the output depends on the present values of inputs as well as previous values of inputs are called ***sequential logic circuits***. Although a logic gate, by itself, has no storage (memory) capability, several gates can be connected together to have storage capability. The most important memory element is the Flip-Flop, which is made up of an assembly of logic gates. A ***Flip-Flop*** (***FF***) is an electronic circuit with two stable states ('0' or '1') that can be used to store binary data. The stored data can be changed by applying various inputs. Flip-Flops and ***latches*** (Flip-Flop with level trigger) are fundamental building blocks of digital electronic systems used in computers, communications, and many other types of systems. Both are used as data storage elements. It is the basic storage element in sequential logic systems.



(a) J-K Flip-Flop

Truth table of NOR gate

Input			Output
J	K	CLK	Q
0	0	↑	Q_0 (No Change)
0	1	↑	0 (Clear)
1	0	↑	1 (Set)
1	1	↑	$\overline{Q}_0$ (Toggle)

(b)

Fig.11-9: J-K flip-flop: (a) Symbol, and (b) truth table

The difference between a latch and a Flip-Flop is that a latch is ***level-triggered*** (outputs can change as soon as the inputs change) and Flip-Flop is ***edge-triggered*** that changes state only when a control signal goes from high to low or low to high). This control signal is called the ***clock signal*** (***CLK***). There are many types of latches and Flip-Flops that are used to design digital systems. But here only the most commonly used ***J-K Flip-Flop*** is described.

Fig.11-9 shows the symbol and truth table of a ***J-K Flip-Flop*** that is triggered by the ***positive-going transition*** (***PGT***) of the CLK signal (when CLK goes HIGH from LOW). The J and K inputs control the output state of the FF. The upward arrows (↑) in

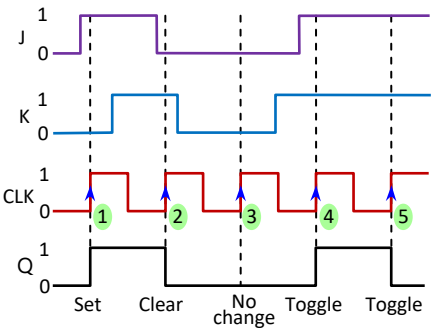


Fig.11-10: Operation process of J-K flip-flop

the truth table indicate positive-going edge of the CLK or active clock. Although a FF has two outputs (Q, and $\bar{Q}$), normally Q is used. When J=0, and K=0, the output state will not change. When J=1, and K=0, the output will be '1' with an active clock. Similarly, when J=0, and K=1, the output will be '0' with an active clock. If J=K=1, the output will toggle on each active clock. Here toggle means, the output will go just opposite to the state it was before the active CLK. The operation of a J-K FF is further illustrated in Fig.11-10. The changes of J, and K with time are shown (violet and blue) in graphs. The active clock pulses (positive going transitions) are shown in red color (1 to 5) and the output of the J-K FF is shown in black color. The initial output was LOW (0). At the first CLK, J=1 and K=0. So the output has been ***SET*** (SET means HIGH, CLEAR means LOW). At the 2nd clock pulse, J=0, K=1, so the output has been cleared (goes to LOW). At 3rd clock J=K=0, so the output has not been changed (remains unchanged). At the 4th and 5th clocks J=K=1, so the output has toggled (goes to opposite state it was before the clock).

Pin Diagrams of Digital ICs

The pin diagrams of fundamental logic gate ICs are given in Fig.11-11. These are 14 pin ICs and are found as 54 series (for military applications) and 7400 series (for normal applications).

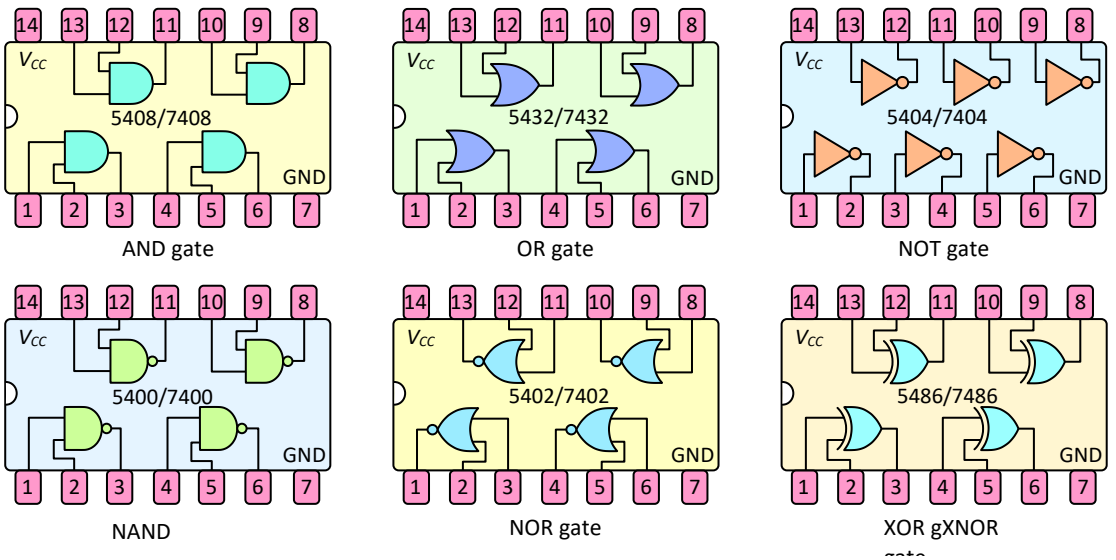


Fig.11-11: Pin diagram of different digital logic gates ICs

References:

[1] Electronic Principles – by Albert Malvino, David Bates

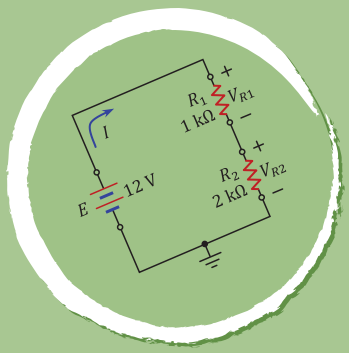
[3] Op-Amps and Linear Integrated Circuits 4th Edition – by Ram Gayakwad

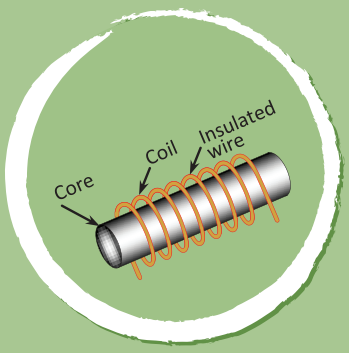
[4] Electronic Devices and Circuit Theory Book – by Louis Nashelsky and Robert Boylestad

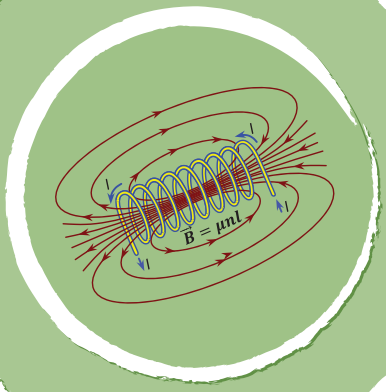
[5] Electronic Devices And Circuits, 5th Eddition – by David A. Bell

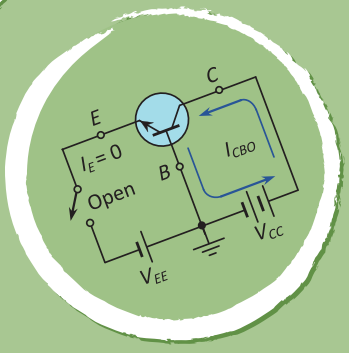
[6] Digital Systems Principles And Applications -by Ronald Tocci

Network of Instrument Technical personnel and User scientists of Bangladesh (NITUB)









Contact Address :
Alishan Complex (2nd Floor, Room No-309)
300, Elephant Road, Dhaka-1205, Bangladesh
Phone : +8802223364136
E-mail : nitub@bangla.net
Web : www.nitub.org